FORM PTO-1390 (REV. 9-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	
NNEX0002	
U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	
Unknown	09/979551

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US00/14768	26 May 2000	27 May 1999

TITLE OF INVENTION
Massively Parallel Interface for Electronic Circuits

APPLICANT(S) FOR DO/EO/US
Chong et al

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [X] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [X] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [ ] Other items or information:

U.S. APPLICATION NO (if known, see 37 CFR 1.5) Unknown	INTERNATIONAL APPLICATION NO PCT/US00/14768	ATTORNEY'S DOCKET NUMBER NNEX0002

21. [X] The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):

	CALCULATIONS PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**	
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**	
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 710.00
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$
Total claims	78 - 20 =	58	x **$18.00**	$ 1,044 00
Independent claims	4 - 3 =	1	x **$84.00**	$ 84 00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$ 0 00
TOTAL OF ABOVE CALCULATIONS			=	$ 1,838 00
[X] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$
SUBTOTAL			=	$ 919 00
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 0.00
TOTAL NATIONAL FEE			=	$ 919 00
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property			+	$ 40.00
TOTAL FEES ENCLOSED			=	$ 959 00
			Amount to be refunded:	$
			charged:	$ 959 00

a. [ ] A check in the amount of $ _____ to cover the above fees is enclosed.

b. [X] Please charge my Deposit Account No. 07-1445 in the amount of $ 959.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 07-1445 . A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO

SIGNATURE

Michael A. Glenn

NAME

30,176

REGISTRATION NUMBER

Rec'd PCT/PTO 21 NOV 2001
PCT/US00/14768
09979551

Massively Parallel Interface for Electronic Circuit

FIELD OF THE INVENTION

The invention relates to the field of integrated circuit (IC) testing and burn-in structures and processes, as well as high bandwidth electronic systems. More particularly, the invention relates to improvements in photolithography-patterned spring contacts and enhanced system interconnect assemblies having photolithography-patterned spring contacts for use in the testing or burn-in of integrated circuits and interconnecting a large number of signals between electronic systems or subsystems.

BACKGROUND OF THE INVENTION

Integrated circuits are typically tested in wafer form (wafer sort) before they are packaged. During wafer sort, integrated circuits are tested one or few at a time, even though there may be hundreds or even hundreds of thousands of the same integrated circuit located on a wafer. The packaged integrated circuits are then tested again, and burned-in, if necessary.

Parallel testing on the wafer level has been limited in number and has so far been limited to low pin count devices, due to the difficulty in managing the large number of interconnects, and the limited amount of electronics which can conventionally be placed close to a wafer under test.

Attempts have also been made to burn-in ICs while in the wafer form. However, wafer-level burn-in is plagued with multiple problems, such as thermal expansion mismatch between the connector and the silicon wafer under test. Conventional structures, such as large area substrates having a large plurality of fanout traces which are electrically connected to pin or socket connectors, are typically implemented to manage connections between the IC under test, test electronics, and power management electronics.

The density of integrated circuits on semiconductor wafers continues to increase, due to semiconductor device scaling, with more gates and memory bits per unit area of silicon. As well, the use of larger semiconductor wafers (*e.g.* often having a nominal diameter 8 inches or 12 inches) has become common. However,

semiconductor test costs have increased on a cost per unit area of silicon basis. Therefore, semiconductor test costs have increased disproportionately over time, to become a greater percentage of the total manufacturing cost for each integrated circuit device.

Furthermore, advances in chip scale packaging (CSP) and other forms of small footprint packages have often made traditional packaged IC handlers obsolete for testing and burn-in.

In some conventional large surface area substrate integrated circuit (IC) test boards, electrical contacts between the test board and an integrated circuit wafer are typically provided by tungsten needle probes. However, tungsten needle probe technology is not able to meet the interconnect requirements of advanced semiconductors having higher pin counts, smaller pad pitches, and higher clock frequencies.

While emerging technologies have provided spring probes for different probing applications, most probes have inherent limitations, such as limited pitch, limited pin count, varying levels of flexibility, limited probe tip geometries, limitations of materials, and high costs of fabrication.

K. Banerji, A. Suppelsa, and W. Mullen III, *Selectively Releasing Conductive Runner and Substrate Assembly Having Non-Planar Areas,* U.S. Patent No. 5,166,774 (24 November 1992) disclose a runner and substrate assembly which comprises "a plurality of conductive runners adhered to a substrate, a portion of at least some of the conductive runners have non-planar areas with the substrate for selectively releasing the conductive runner from the substrate when subjected to a predetermined stress".

A. Suppelsa, W. Mullen III and G. Urbish, *Selectively Releasing Conductive Runner and Substrate Assembly,* U.S. Patent No. 5,280,139 (18 January 1994) disclose a runner and substrate assembly which comprises "a plurality of conductive runners adhered to a substrate, a portion of at least some of the conductive runners have a lower adhesion to the substrate for selectively releasing the conductive runner from the substrate when subjected to a predetermined stress".

D. Pedder, *Bare Die Testing,* U.S. Patent No. 5,786,701 (28 July 1998) disclose a testing apparatus for testing integrated circuits (ICs) at the bare die stage, which includes "a testing station at which microbumps of conductive material are located on interconnection trace terminations of a multilayer interconnection structure, these terminations being distributed in a pattern corresponding to the pattern of contact pads on the die to be tested. To facilitate testing of the die before separation from a wafer using the microbumps, the other connections provided to and from the interconnection structure have a low profile".

D. Grabbe, I. Korsunsky and R. Ringler, *Surface Mount Electrical Connector,* U.S. Patent No. 5,152,695 (06 October 1992) disclose a connector for electrically connecting a circuit between electronic devices, in which "the connector includes a platform with cantilevered spring arms extending obliquely outwardly therefrom. The spring arms include raised contact surfaces and in one embodiment, the geometry of the arms provide compound wipe during deflection".

H. Iwasaki, H. Matsunaga, and T. Ohkubo, *Partly Replaceable Device for Testing a Multi-Contact Integrated Circuit Chip Package,* U.S. Patent No. 5,847,572 (08 December 1998) disclose "a test device for testing an integrated circuit (IC) chip having side edge portions each provided with a set of lead pins. The test device comprises a socket base, contact units each including a contact support member and socket contact numbers, and anisotropic conductive sheet assemblies each including an elastic insulation sheet and conductive members. The anisotropic conductive sheet assemblies are arranged to hold each conductive member in contact with one of the socket contact members of the contact units. The test device further comprises a contact retainer detachably mounted on the socket base to bring the socket contact members into contact with the anisotropic sheet assemblies to establish electrical communication between the socket contact members and the conductive members of the anisotropic conductive sheet assemblies. Each of the contact units can be replaced by a new contact unit if the socket contact members partly become fatigued, thereby making it possible to facilitate the maintenance of the test device. Furthermore, the lead pins of the IC chip can be electrically connected to a test circuit board with the shortest paths formed by part of the socket contact members and the conductive members of the anisotropic conductive sheet assemblies".

W. Berg, *Method of Mounting a Substrate Structure to a Circuit Board,* U.S. Patent No. 4,758,9278 (19 July 1988) discloses "a substrate structure having contact pads is mounted to a circuit board which has pads of conductive material exposed at one main face of the board and has registration features which are in predetermined positions relative to the contact pads of the circuit board. The substrate structure is provided with leads which are electrically connected to the contact pads of the substrate structure and project from the substrate structure in cantilever fashion. A registration element has a plate portion and also has registration features which are distributed about the plate portion and are engageable with the registration features of the circuit board, and when so engaged, maintain the registration element against movement parallel to the general plane of the circuit board. The substrate structure is attached to the plate portion of the registration element so that the leads are in predetermined position relative to the registration features of the circuit board, and in this position of the registration element the leads of the substrate structure overlie the contact pads of the circuit board. A clamp member maintains the leads in electrically conductive pressure contact with the contact pads of the circuit board".

D. Sarma, P. Palanisamy, J. Hearn and D. Schwarz, *Controlled Adhesion Conductor,* U.S. Patent No. 5,121,298 (09 June 1992) disclose "Compositions useful for printing controllable adhesion conductive patterns on a printed circuit board include finely divided copper powder, a screening agent and a binder. The binder is designed to provide controllable adhesion of the copper layer formed after sintering to the substrate, so that the layer can lift off the substrate in response to thermal stress. Additionally, the binder serves to promote good cohesion between the copper particles to provide good mechanical strength to the copper layer so that it can tolerate lift off without fracture".

R. Mueller, *Thin-Film Electrothermal Device,* U.S. Patent No. 4,423,401 (27 December 1983) discloses " A thin film multilayer technology is used to build micro-miniature electromechanical switches having low resistance metal-to-metal contacts and distinct on-off characteristics. The switches, which are electrothermally activated, are fabricated on conventional hybrid circuit substrates using processes compatible with those employed to produce thin-film circuits. In a preferred form, such a switch includes a cantilever actuator member comprising a resiliently bendable strip of a hard insulating material (*e.g.* silicon nitride) to which

a metal (*e.g.* nickel) heating element is bonded. The free end of the cantilever member carries a metal contact, which is moved onto (or out of) engagement with an underlying fixed contact by controlled bending of the member via electrical current applied to the heating element".

S. Ibrahim and J. Elsner, *Multi-Layer Ceramic Package*, U.S. Patent No. 4,320,438 (16 March 1982) disclose "In a multi-layer package, a plurality of ceramic lamina each has a conductive pattern, and there is an internal cavity of the package within which is bonded a chip or a plurality of chips interconnected to form a chip array. The chip or chip array is connected through short wire bonds at varying lamina levels to metallized conductive patterns thereon, each lamina level having a particular conductive pattern. The conductive patterns on the respective lamina layers are interconnected either by tunneled through openings filled with metallized material, or by edge formed metallizations so that the conductive patterns ultimately connect to a number of pads at the undersurface of the ceramic package mounted onto a metalized board. There is achieved a high component density; but because connecting leads are "staggered" or connected at alternating points with wholly different package levels, it is possible to maintain a 10 mil spacing and 10 mil size of the wire bond lands. As a result, there is even greater component density but without interference of wire bonds one with the other, this factor of interference being the previous limiting factor in achieving high component density networks in a multi-layer ceramic package".

F. McQuade, and J. Lander, *Probe Assembly for Testing Integrated Circuits*, U.S. Patent No. 5,416,429 (16 May 1995) disclose a probe assembly for testing an integrated circuit, which "includes a probe card of insulating material with a central opening, a rectangular frame with a smaller opening attached to the probe card, four separate probe wings each comprising a flexible laminated member having a conductive ground plane sheet, an adhesive dielectric film adhered to the ground plane, and probe wing traces of spring alloy copper on the dielectric film. Each probe wing has a cantilevered leaf spring portion extending into the central opening and terminates in a group of aligned individual probe fingers provided by respective terminating ends of said probe wing traces. The probe fingers have tips disposed substantially along a straight line and are spaced to correspond to the spacing of respective contact pads along the edge of an IC being tested. Four spring clamps each have a cantilevered portion which contact the leaf spring portion of a respective probe wing, so as to

provide an adjustable restraint for one of the leaf spring portions. There are four separate spring clamp adjusting means for separately adjusting the pressure restraints exercised by each of the spring clamps on its respective probe wing. The separate spring clamp adjusting means comprise spring biased platforms each attached to the frame member by three screws and spring washers so that the spring clamps may be moved and oriented in any desired direction to achieve alignment of the position of the probe finger tips on each probe wing".

D. Pedder, *Structure for Testing Bare Integrated Circuit Devices,* European Patent Application No. EP 0 731 369 A2 (Filed 14 February 1996), U.S. Patent No. 5,764,070 (09 June 1998) discloses a test probe structure for making connections to a bare IC or a wafer to be tested, which comprises "a multilayer printed circuit probe arm which carries at its tip an MCM-D type substrate having a row of microbumps on its underside to make the required connections. The probe arm is supported at a shallow angle to the surface of the device or wafer, and the MCM-D type substrate is formed with the necessary passive components to interface with the device under test. Four such probe arms may be provided, one on each side of the device under test".

B. Eldridge, G. Grube, I. Khandros, and G. Mathieu, *Method of Mounting Resilient Contact Structure to Semiconductor Devices,* U.S. Patent No. 5,829,128 (03 November 1998), *Method of Making Temporary Connections Between Electronic Components,* U.S. Patent No. 5,832,601 (10 November 1998), *Method of Making Contact Tip Structures,* U.S. Patent No. 5,864,946 (02 February 1999), *Mounting Spring Elements on Semiconductor Devices,* U.S. Patent No. 5,884,398 (23 March 1999), *Method of Burning-In Semiconductor Devices,* U.S. Patent No. 5,878,486 (09 March 1999), and *Method of Exercising Semiconductor Devices,* U.S. Patent No. 5,897,326 (27 April 1999), disclose "Resilient contact structures are mounted directly to bond pads on semiconductor dies, prior to the dies being singulated (separated) from a semiconductor wafer. This enables the semiconductor dies to be exercised (*e.g.* tested and/or burned-in) by connecting to the semiconductor dies with a circuit board or the like having a plurality of terminals disposed on a surface thereof. Subsequently, the semiconductor dies may be singulated from the semiconductor wafer, whereupon the same resilient contact structures can be used to effect interconnections between the semiconductor dies and other electronic components (such a wiring substrates, semiconductor packages, etc.).

Using the all-metallic composite interconnection elements of the present invention as the resilient contact structures, burn-in can be performed at temperatures of at least 150° C., and can be completed in less than 60 minutes". While the contact tip structures disclosed by B. Eldridge et al. provide resilient contact structures, the structures are each individually mounted onto bond pads on semiconductor dies, requiring complex and costly fabrication. As well, the contact tip structures are fabricated from wire, which often limits the resulting geometry for the tips of the contacts. Furthermore, such contact tip structures have not been able to meet the needs of small pitch applications (*e.g.* typically on the order of 50 µm spacing for a peripheral probe card, or on the order of 75 µm spacing for an area array).

T. Dozier II, B. Eldridge, G. Grube, I. Khandros, and G. Mathieu, *Sockets for Electronic Components and Methods of Connecting to Electronic Components,* U.S. Patent No. 5,772,451 (30 June 1998) disclose "Surface-mount, solder-down sockets permit electronic components such as semiconductor packages to be releaseably mounted to a circuit board. Resilient contact structures extend from a top surface of a support substrate, and solder-ball (or other suitable) contact structures are disposed on a bottom surface of the support substrate. Composite interconnection elements are used as the resilient contact structures disposed atop the support substrate. In any suitable manner, selected ones of the resilient contact structures atop the support substrate are connected, via the support substrate, to corresponding ones of the contact structures on the bottom surface of the support substrate. In an embodiment intended to receive an LGA-type semiconductor package, pressure contact is made between the resilient contact structures and external connection points of the semiconductor package with a contact force which is generally normal to the top surface of the support substrate. In an embodiment intended to receive a BGA-type semiconductor package, pressure contact is made between the resilient contact structures and external connection points of the semiconductor package with a contact force which is generally parallel to the top surface of the support substrate".

Other emerging technologies have disclosed probe tips on springs which are fabricated in batch mode processes, such as by thin-film or micro electronic mechanical system (MEMS) processes.

D. Smith and S. Alimonda, *Photolithographically Patterned Spring Contact,* U.S. Patent No. 5,613,861 (25 March 1997), U.S. Patent No. 5,848,685 (15 December 1998), and International Patent Application No. PCT/US 96/08018 (Filed 30 May 1996), disclose a photolithography patterned spring contact, which is "formed on a substrate and electrically connects contact pads on two devices. The spring contact also compensates for thermal and mechanical variations and other environmental factors. An inherent stress gradient in the spring contact causes a free portion of the spring to bend up and away from the substrate. An anchor portion remains fixed to the substrate and is electrically connected to a first contact pad on the substrate. The spring contact is made of an elastic material and the free portion compliantly contacts a second contact pad, thereby contacting the two contact pads". While the photolithography patterned springs, as disclosed by Smith et al., are capable of satisfying many IC probing needs, the springs are small, and provide little vertical compliance to handle the planarity compliance needed in the reliable operation of many current IC prober systems. Vertical compliance for many probing systems is typically on the order of 0.004" - 0.010", which often requires the use of tungsten needle probes.

The round trip transit time between the a device under test and conventional test equipment is often longer then the stimulus to response times of high speed electronic circuits. It would be advantageous to provide a test interface system which reduces this transit time, by placing high speed test electronics in close proximity of the device under test, while meeting space and cost constraints. Furthermore, it would be advantageous to provide a test interface system which minimizes the cost, complexity, tooling, and turn around time required to change the test structure for the testing of different devices. The development of such a system would constitute a major technological advance.

It would be advantageous to provide a test interface system which provides probe contact with many, hundreds, or even hundreds of thousands of pads for one or more devices on a semiconductor wafer, such as for massively parallel testing and/or burn-in applications, wherein the pads may be in close proximity of one another, with a minimum spacing approaching 1 mil or less, while providing a uniform force across all probes over the entire wafer. It would also be advantageous to provide such a test interface system which organizes and manages the interconnections between the device under test and the tester electronics, while maintaining signal integrity and power and ground stability, and

assures that no two or more adjacent pads are contacted by a single test probe tip. Furthermore, it would be advantageous to provide such a test structure which preferably provides planarity compliance with the devices under test. The development of such a system would constitute a further technological advance.

In addition, it would be advantageous to provide such a test system which preferably provides continuous contact with many, hundreds, or even hundreds of thousands of pads for one or more devices on a semiconductor wafer over a wide temperature range, while providing thermal isolation between the test electronics and the devices under test. As well, it would be advantageous to provide a system for separate thermal control of the test system and of the devices under test.

It would also be advantageous to provide a test interface system which may be used to detect power to ground shorts in any die quickly, and to isolate power from a die having a detected power to ground short, before damage is done to the test electronics. In addition, it would be advantageous to provide a test interface structure which can detect that the contacts to many, hundreds, or even hundreds of thousands of pads are reliably made and are each of the contacts are within the contact resistance specification, to assure that the self inductance and self capacitance of each signal line are below values that would adversely affect test signal integrity, and to assure that the mutual inductance and mutual capacitance between pairs of signal lines and between signal lines and power or ground lines are below values that would adversely affect test signal integrity. As well, it would also be advantageous to provide a test interface structure which provides stimulus and response detection and analysis to many, hundreds, or even hundreds of thousands, of die under test in parallel, and which preferably provides diagnostic tests to a failed die, in parallel with the continued testing of all other die.

Furthermore, it would be advantageous to provide a large array interface system which can reliably and repeatedly establish contact to many, hundreds, or even hundreds of thousands of pads, without the need to periodically stop and inspect and/or clean the probe interface structure.

It would also be advantageous to provide a system for massively parallel interconnections between electrical components, such as between computer

systems, which utilize spring probes within the interconnection structure, to provide high pin counts, small pitches, cost-effective fabrication, and customizable spring tips. The development of such a method and apparatus would constitute a major technological advance.

SUMMARY OF THE INVENTION

Several embodiments of massively parallel interface integrated circuit test assemblies are disclosed, which use one or more substrates to establish connections between one or more integrated circuits on a semiconductor wafer, and use one or more test modules which are electrically connected to the integrated circuits on the semiconductor wafer through the substrates. One or more layers on the intermediate substrates preferably include MEMS and/or thin-film fabricated spring probes. The massively parallel interface assemblies provide tight pad pitch and compliance, and preferably enable the parallel testing or burn-in of multiple ICs. In some preferred embodiments, the massively parallel interface assembly structures include separable standard electrical connector components, which reduces assembly manufacturing cost and manufacturing time. These massively parallel interface structures and assemblies enable high speed testing in wafer form, and allow test electronics to be located in close proximity to the wafer. Preferred embodiments of the massively parallel interface assemblies provide thermal expansion matching to the wafer under test, and provide a thermal path for system electronic. Alternate massively parallel interface structures provide massively parallel connection interfaces, which may be used in a wide variety of circuitry, such as for interconnecting computers in a network, or for interconnecting other electronic circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a plan view of a linear array of photolithographically patterned springs, prior to release from a substrate;

Figure 2 is a perspective view of a linear array of photolithographically patterned springs, after release from a substrate;

Figure 3 is a side view of a first, short length photolithographically patterned spring, having a first effective radius and height after the short length spring is released from a substrate;

Figure 4 is a side view of a second, long length photolithographically patterned spring, having a second large effective radius and height after the long length spring is released from a substrate;

Figure 5 is a perspective view of opposing photolithographic springs, having an interleaved spring tip pattern, before the springs are released from a substrate;

Figure 6 is a perspective view of opposing photolithographic springs, having an interleaved spring tip pattern, after the springs are released from a substrate;

Figure 7 is a top view of a first opposing pair of interleaved multiple-point photolithographic spring probes, in contact with a single trace on an integrated circuit device, and a second opposing pair of interleaved multiple-point photolithographic spring probes, in contact with a single pad on the integrated circuit device;

Figure 8 is a plan view of opposing single-point photolithographic spring probes, before the springs are released from a substrate;

Figure 9 is a top view of parallel and opposing single-point photolithographic spring probes, after the springs are released from a substrate, in contact with a single pad on an integrated circuit device;

Figure 10 is a front view of a shoulder-point photolithographic spring probe;

Figure 11 is a partial cross-sectional side view of a shoulder-point photolithographic spring in contact with a trace on an integrated circuit device;

Figure 12 is a perspective view of a multiple shoulder-point photolithographic spring probe;

Figure 13 is a partial cross-sectional view of a multi-layered spring probe substrate providing controlled impedance and integrated components;

Figure 14 is a partial plan view of a substrate, in which a plurality of trace distribution regions are defined on the probe surface of the substrate, between a plurality of spring probes and a plurality of via contacts;

Figure 15 is a partial cutaway assembly view of a massively parallel test assembly having test electronics located in close proximity to the wafer under test;

Figure 16 is a partial perspective view of a massively parallel interconnection assembly;

Figure 17 is a partial expanded cross-sectional view of a massively parallel test assembly having an intermediate system board, which shows staged pitch and distribution across a substrate, a system board, and a flex circuit having a pad matrix;

Figure 18 is an expanded layer plan view of a wafer, a circular substrate, and a rectangular system board;

Figure 19 is an expanded layer plan view of a wafer, a plurality of rectangular substrates, and a rectangular system board;

Figure 20 is a partial cross-sectional view of one embodiment of the flexible circuit structure;

Figure 21 is a partial cross-sectional view of an alternate embodiment of the flexible circuit, which comprises a flex circuit membrane structure;

Figure 22 is a partial perspective view of a flexible membrane circuit structure, wherein a flexible region is defined as an extension of the electronic test card structure;

Figure 23 is a partial perspective view of an alternate flexible circuit structure, wherein a flexible circuit is attached to an electronic test card structure;

Figure 24 is a partial cross-sectional view of one embodiment of a preferred flex circuit region of a test electronics module, in which the flex circuit is wrapped around the power and ground buss structure, and which preferably includes a thermal path across the flex circuit between a power module and a buss bar;

Figure 25 is a partial cross-sectional view of an alternate embodiment of the flex circuit region of a test electronics module, in which a plurality of power modules mounted on the inner surface of a flex circuit are positioned in thermal contact with a plurality of buss bars;

Figure 26 is a partial cross-sectional view of a second alternate embodiment of the flex circuit region of a test electronics module, in which a power module is electrically connected to the outer surface of a flex circuit, and is positioned in thermal contact with a buss bar;

Figure 27 is a perspective view of an alternate embodiment of a test electronics module, in which an integrated module base provides a pad matrix on a first planar region, and in which a power module is electrically connected to the pad matrix and to one or more buss bars, and is positioned in thermal contact with a buss bar;

Figure 28 is a partial cutaway assembly view of an alternate massively parallel test assembly having an intermediate system board, in which flexible spring probes are located on the lower surface of the system board;

Figure 29 is a partial cutaway assembly view of another alternate massively parallel test assembly having an intermediate system board, in which an interposer structure provides electrical connections between the substrate and the system board;

Figure 30 is a partial cutaway assembly view of a basic massively parallel test assembly, in which a substrate having spring probes is directly connected to the test electronics modules;

Figure 31 is a partial expanded cross-sectional view of a basic massively parallel test assembly, which shows staged pitch and distribution across a substrate and a flex circuit having a pad matrix;

Figure 32 is a partial cutaway assembly view of a massively parallel burn-in test assembly, in which burn-in test modules are connected directly to the system board, and in which separate temperature control systems are provided for the wafer under test and for the test electronics modules;

Figure 33 is a first partial expanded cross-sectional view showing massively parallel test assembly and alignment hardware and procedures;

Figure 34 is a second partial expanded cross-sectional view showing massively parallel test assembly and alignment hardware and procedures;

Figure 35 is a partial schematic block diagram of test circuitry for the massively parallel test system;

Figure 36 is a partial cutaway assembly view of a massively parallel interface assembly, in which a plurality of interface modules are connected, through a plurality of probe spring interposers and a system interconnect board structure;

Figure 37 is a partial cutaway assembly view of an alternate massively parallel interface assembly, in which a plurality of interface modules are connected through a system board and a system interconnect board structure;

Figure 38 is a schematic block diagram of connections between a plurality of computer systems, using a massively parallel interface assembly; and

Figure 39 is a schematic block diagram of connections between a plurality of electronic circuits, using a massively parallel interface assembly.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 is a plan view 10 of a linear array 12 of photolithographically patterned springs 14a-14n, prior to release from a substrate 16. The conductive springs 14a-14n are typically formed on the substrate layer 16, by successive layers of deposited metal 17 (*e.g.* such as layers 17a,17b in FIG. 13), such as through low and high energy plasma and sputter deposition processes, followed by photolithographic patterning, as is widely known in the semiconductor industry.

The successive layers 17 have different inherent levels of stress. The release regions 18 of the substrate 16 are then processed by undercut etching, whereby portions of the spring contacts 14a-14n, which are located over the release regions 18, are released from the substrate 16 and extend (*i.e.* bend) away from the substrate 16, as a result of the inherent stresses between the deposited metallic layers. Fixed regions 15 (FIG. 3, FIG. 4) of the deposited metal traces remain affixed to the substrate 16, and are typically used for routing (*i.e.* such as for redistribution or fan-out) from the spring contacts 14a-14n. Figure 2 is a perspective view 22 of a linear array 12 of photolithographically patterned springs 14a-14n, after release from a substrate 16. The spring contacts 14a-14n may be formed in high density arrays, with a fine pitch 20, currently on the order of 0.001 inch.

Figure 3 is a side view 26a of a first photolithographically patterned spring 14 having a short length 28a, which is formed to define a first effective spring angle 30a (which can be from a few degrees to a full circle), spring radius 31a, and spring height 32a, after the patterned spring 14 is released from the release region 18a of the substrate 16, away from the planar anchor region 15. Figure 4 is a side view 26b of a second photolithographically patterned spring 14, having a long spring length 28b, which is formed to define a second large effective spring angle 30b, spring radius 31b and spring height 32b, after the patterned spring 14 is released from the release region 18b of the substrate 16. The effective geometry of the formed spring tips 14 is highly customizable, based upon the intended application. As well, the spring tips are typically flexible, which allows them to be used for many applications.

Patterned spring probes 14 are capable of very small spring to spring pitch 20, which allows multiple spring probes 14 to be used to contact power or ground pads on an integrated circuit device 44 (FIG. 18, FIG. 19), thereby improving current carrying capability. As well, for a massively parallel interconnect assembly 78 (*e.g.* 78a, FIG. 15) having an array 12 (FIG. 1) of spring probes 14, multiple spring probes 14 may be used to probe I/O pads 47 on an IC substrate 48 (FIG. 9), such as on an integrated circuit device under test (DUT) 44 (FIG. 18, FIG. 19). Every spring probe contact 14 to be verified for continuity after engagement of the spring contacts 14 to the wafer 104 under test (FIG. 15), thereby ensuring complete electrical contact between a massively parallel

interface assembly 78 and a devices 44 on a wafer 104 (FIG. 15), before testing procedures begin.

Improved Structures for Miniature Springs. Figure 5 is a first perspective view of opposing photolithographic springs 34a,34b, having an interleaved spring tip pattern, before spring to substrate detachment. Figure 6 is a perspective view of opposing interleaved photolithographic springs 34a, 34b, after spring to substrate detachment.

The interleaved photolithographic springs 34a, 34b each have a plurality of spring contact points 24. When spring contacts are used for connection to power or ground traces 46 or pads 47 of an integrated circuit device 44, the greatest electrical resistance occurs at the point of contact. Therefore, an interleaved spring contact 34, having a plurality of contact points 24, inherently lowers the resistance between the spring contact 34 and a trace 46 or pad 47. As described above, multiple interleaved spring probes 34 may be used for many applications, such as for high quality electrical connections for an integrated circuit device 44, or for a massively parallel interface assembly 78 (FIG. 15), such as for probing an integrated circuit device 44 during testing.

Figure 7 is a top view 42 of opposing interleaved photolithographic spring pairs 34a,34b in contact with the same traces 46 or pads 47 on an integrated circuit device under test (DUT) 44. The interleaved spring contact pair 34a and 34b allows both springs 34a and 34b, each having a plurality of contact points 24, to contact the same trace 46 or pad 47. As shown in Figure 5, when a zig-zag gap 38 is formed between the two springs 34a,34b on a substrate 16, multiple tips 24 are established on each spring 34a,34b. Before the interleaved spring probes 34a,34b are released from the substrate 16, the interleaved points 24 are located within an overlapping interleave region 36. When the interleaved spring probes 34a,34b are released from the substrate 16, the interleaved spring points 24 remain in close proximity to each other, within a contact region 40, which is defined between the springs 34a, 34b. The interleaved spring contact pair 34a and 34b may then be positioned, such that both interleaved spring probes 34a and 34b contact the same trace 46, such as for a device under test 44, providing increased reliability. As well, since each interleaved spring 34a,34b includes multiple spring points 24, contact with a trace 46 is

increased, while the potential for either overheating or current arcing across the multiple contact points 24 is minimized.

Figure 8 is a top view of parallel and opposing single-point photolithographic springs 14, before the springs 14 are released from a substrate 16. As described above for interleaved springs 34a, 34b, parallel springs 14 may also be placed such that the spring tips 24 of multiple springs contact a single trace 46 on a device 44. As well, opposing spring probes 14 may overlap each other on a substrate 16, such that upon release from the substrate 16 across a release region 18, the spring tips 24 are located in close proximity to each other. Figure 9 is a top view of parallel and opposing parallel single-point photolithographic springs 14, after the springs 14 are released from the substrate 16, wherein the parallel and opposing parallel single-point photolithographic springs 14 contact a single pad 47 on an integrated circuit device 44.

Figure 10 is a front view of a shoulder-point photolithographic spring 50, having a point 52 extending from a shoulder 54. Figure 11 is a partial cross-sectional side view of a shoulder-point photolithographic spring 50, in contact with a trace 46 on an integrated circuit device. Figure 12 is a perspective view of a multiple shoulder-point photolithographic spring 50. Single point spring probes 14 typically provide good physical contact with conductive traces 46 on an integrated circuit device 22, often by penetrating existing oxide layers on traces 46 or pads 47 by a single, sharp probe tip 24. However, for semiconductor wafers 104 or integrated circuit devices having thin or relatively soft traces 46 or pads 47, a single long probe tip 24 may penetrate beyond the depth of the trace 46, such as into the IC substrate 48, or into other circuitry.

Shoulder-point photolithographic springs 50 therefore include one or more extending points 52, as well as a shoulder 54, wherein the points 52 provide desired penetration to provide good electrical contact to traces 46, while the shoulder 54 prevents the spring 50 from penetrating too deep into a device 44 or wafer 104. Since the geometry of the spring probes 50 are highly controllable by photolithographic screening and etching processes, the detailed geometry of the shoulder-point photolithographic spring 50 is readily achieved.

Figure 13 shows a partial cross-sectional view 56 of an ultra high frequency spring probe substrate 16. For embodiments wherein a spring probe 61 and related

electrical conductors 60, 68, 64 on and through the substrate 16 are required to be impedance matched, one or more conductive reference surfaces 58a,58b,58c,58d and vias 65a,65b,65c may preferably be added, either within or on the substrate 16. The substrate 16 may also contain alternating ground reference traces 62a,62b, which are connected to reference planes 58a,58b,58c, to effectively provide a shielded coaxial transmission line environment 63. As well, the impedance control surfaces 58a,58b,58c,58d are not limited to the planar surfaces shown in Figure 13.

An insulating layer 66 may be deposited on a portion the probe spring 61, such as on the fixed region of the probe spring 61, up to but not enclosing the tip 24 (FIG. 2), as well as on the trace 60, which connects the spring probe 61 to the via 68. A conductive layer 58d may be deposited on top of the insulating layer 66, to provide a coaxial, controlled low impedance connection. Alternate layers of conductive materials 58 and dielectric materials 66 can preferably be integrated within the substrate 16, such as for embodiments which require decoupling capacitors in close proximity to a probe spring 61. For a substrate 16 which is a conductive material, such as silicon, a thin oxide layer 57 may preferably be deposited between the substrate 16 and a conductive reference plane 58c, thereby forming a high capacitance structure 59 between the spring probe 61 and the ground planes 58a and 58b. As well, one or more assembled components 69, such as passive components 69 (*e.g.* typically capacitors, resistors, and/or inductors), or active component devices 69, may be incorporated on either surface 62a,62 of the substrate.

The fixed portions 15 of the spring probes 61 typically extend a relatively short distance across the substrate 16. Traces 60 located on the surface of the substrate 16 are electrically connected to the fixed portions 15 of the spring probes 61, and electrically connect the probe springs 61 to the vias 68. The traces may be comprised of a different material than the spring probes 61, and are preferably comprised of metals having high electrical conductivity (*e.g.* such as copper or gold).

Figure 14 is a partial plan view 72 of a substrate 16, in which a plurality of distribution fanout traces 60 are defined on the probe surface 62a of the substrate 16, between a plurality of spring probes 61 and a plurality of via contacts 70. As described above, the spring probes 61, which are preferably

photolithographically formed springs 61, may currently be formed with a pitch of approximately 0.001 inch. The traces 60 are preferably routed on the probe surface 62a, to connect to via contact areas 70, which are preferably laid out in a matrix across the surface of the substrate 16. In the substrate 16 shown in Figure 14, the via contact areas 70 are positioned with a probe surface first distribution pitch 74a, and a probe surface second distribution pitch 74b.

As the size and design of integrated circuit devices 44 becomes increasingly small and complex, the fine pitch 20 (FIG. 2) provided by miniature spring probe tips 61 becomes increasingly important. Furthermore, with the miniaturization of both integrated circuits 44 and the required test assemblies, differences in planarity between one or more integrated circuits 44 located on a wafer 104 and a substrate 16 containing a large number of spring probes 61 becomes critical.

As seen in Figure 14, lower standoffs 75 are preferably provided on the probe surface 62a of the substrate 16, such as to prevent the substrate 16 from damaging a wafer under test 104, or to set the spring probe tips 24 to operate at an optimal contact angle. The lower standoffs 75 are preferably made of a relatively soft material, such as polyamide, to avoid damage to the semiconductor wafer under test 104. In addition, to further avoid damage to active circuits 44 in the semiconductor wafer 104, the standoffs 75 are preferably placed, such that when the massively parallel interface assembly 78 is aligned with a device 44 on a semiconductor wafer 104, the standoffs 75 are aligned with the saw streets 136 (FIG. 18, FIG. 19) on the semiconductor wafer 104, where there are no active devices 44 or test structures. Furthermore, the height of the lower standoffs 75 are preferably chosen to limit the maximum compression of the spring probes 61a-61n, thus preventing damage to the spring probes 61a-61n.

The substrate 16 also typically includes one or more alignment marks 77 (FIG. 14), preferably on the probe surface 62a, such that the probe surface 62a of the substrate 16 may be precisely aligned with a wafer to be tested 104.

Massively Parallel Interface Assemblies for Testing and Burn-In. Figure 15 is a partial expanded cross-sectional view of a massively parallel test assembly 78a having an intermediate system board 82. Figure 16 is a partial

perspective view 110 of a massively parallel interface assembly 78a. Figure 17 is a partial expanded cross-sectional view 120 of a massively parallel test assembly 78a having an intermediate system board 82, which shows staged pitch and distribution across a substrate 16, a system board 82, and a flex circuit 90 having a pad matrix 88 (FIG. 15) of electrical connectors 119a-119n. As shown in Figure 15 and Figure 17, the interface assembly 78a is typically positioned in relation to a semiconductor wafer 104, having one or more integrated circuits 44, which are typically separated by saw streets 136 (FIG. 18, FIG. 19).

The massively parallel interface assembly 78a provides electrical interconnections to a substrate 16, which may contain hundreds of thousands of spring probe tips 61a-61n, while providing adequate mechanical support for the interface assembly 78a, to work effectively in a typical integrated circuit testing environment. The interface assembly 78a is readily used for applications requiring very high pin counts, for tight pitches, or for high frequencies. As well, the interface assembly 78a is easily adapted to provide electrical contact for all traces 46 (FIG. 7) and input and output pads 47 (FIG. 7, FIG. 9) for one or more integrated circuit devices under test 44 on a wafer 104.

As seen in Figure 15, a plurality of electrically conductive spring probe tips 61a-61n are located on the lower probe surface 62a of the substrate 16, and are typically arranged with a fine spring pitch 20 (FIG. 1, FIG. 17), which is typically required to interconnect to specific pads 47 (FIG. 17) on one or more devices under test 44 on a wafer 104. The spring probe tips 61a-61n may have a variety of tip geometries, such as single point springs 14, interleaved springs 34, or shoulder point springs 50, and are fabricated on the substrate 16, typically using thin-film or MEMS processing methods, to achieve low manufacturing cost, well controlled uniformity, very fine pad pitches 20, and large pin counts. In some embodiments, the flexible connections 64a-64n are built in compliance to photolithographic springs, such as described above, or as disclosed in either U.S. Patent No. 5,848,685 or U.S. Patent No. 5,613,861, which are incorporated herein by reference. The spring probes 61a-61n on the probe side 62a of the substrate 16 mate with pads 47 on each die 44 of the wafer 104.

The fixed trace portions 15,60 (FIG. 3, FIG. 14) are then preferably routed to a plurality of metalized vias 68a-68n, which are typically arranged with a substrate

distribution pitch 74a,74b, such that the vias 68a-68n are preferably distributed relatively uniformly across the substrate 16. Electrically conductive traces 60 are preferably fabricated on one or both sides of the substrate 16, preferably providing a distribution of the conductive connections 64a-64n across the connector surface 62b of the substrate 16.

The probe tips 61a-61n are electrically connected to the electrically conductive connections 64a-64n, preferably through metalized vias 68a-68n within the substrate 16. Each of the plurality of electrically conductive connections 64a-64n are then electrically connected to a plurality of conductive pads 84a-84n on the lower surface 139a on a system board 82. The preferred metallized via electrical connections 68a-68n (*e.g.* such as produced by Micro Substrate Corporation, of Tempe, Arizona) within the substrate 16, are typically fabricated using standard PTH methods, or extrusion methods, such as by first creating holes in the substrate 16, using laser or other drilling methods. The holes are then filled or plated with conductive material, such as by plating or by extrusion. After the conductive vias 68a-68n are formed, they are typically polished back, to provide a flat and smooth surface. Capacitors may preferably be mounted or built into the substrate 16 (FIG. 13), providing close proximity de-coupling to the IC wafer 104 under test.

The substrate 16 is preferably comprised of silicon, glass, ceramic, ceramic glass, or other suitable substrate material, and preferably has a thermal coefficient of expansion (TCE) which matches the thermal coefficient of expansion (TCE) of the wafer 104. In some preferred embodiments of the parallel interface assembly 78, the substrate 16 is relatively thin, such that the substrate 16, the spring probes 61a-61n, and the preferred flexible connections 64a-64n provide enhanced planarity compliance to a wafer under test 104.

In an alternate embodiment of the substrate 16, a starting substrate 16 (*e.g.* such as a silicon substrate 16), is etched, such as by a plasma etching process or a wet anisotropic etching process, to create through holes (*i.e.* vias) in the substrate 16, as practiced in the MEMS industry. The substrate 16 may be thinned, such as by atmospheric plasma ion etching, prior to the creation of the through holes, such that fine pitch holes may be defined in the preferred silicon wafer 16, thereby creating a flexible substrate 16. The flexible substrate 16 is compliant to the surface of one or more devices under test 44 on a wafer 104, such as when a

pressure differential (as described in reference to Figure 32) is provided between the probe surface 62a and the connector surface 62b of the substrate 16. As described above, the holes are then filled or plated with conductive material, such as by plating or by extrusion. After the conductive vias 68a-68n are formed, they are typically polished back, to provide a flat and smooth surface. Capacitors may preferably be mounted or built into the substrate 16 (FIG. 13), providing close proximity de-coupling to the IC wafer 104 under test.

The electrically conductive connections 64a-64n are located on the upper connector surface 62b of the substrate 16, and are connected to the vias 68a-68n. The electrically conductive connections 64a-64n are typically arranged with a connection pitch 122 (FIG. 17), which may be aligned with the substrate distribution pitch 74a,74b, or may preferably be redistributed on the upper connector surface 62b of the substrate 16. In some preferred embodiments of the substrate 16, the electrically conductive connections 64a-64n are preferably distributed relatively uniformly across the substrate 16.

The electrically conductive connections 64a-64n are preferably arranged within an area array, having an array pitch 122 such as 0.5 mm, 1.00 mm or 1.27 mm, which provides a reasonable density to mate to plated through-holes (PTH) 86a-86n on the system board 82 (which are typically arranged with a system board pitch 126), and allows the distribution of signals on multiple layers within the system board 82, without resorting to advanced system boards 82 containing blind conductive vias 86a-86n.

The electrically conductive connections 64a-64n, which contact conductive pads 84a-84n on the underside of the system board 82, maintain electrical connection between the substrate 16 and the system board 82. The electrically conductive connections 64a-64n also provide lateral compliance between a substrate 16 and a system board 82 having different thermal coefficients of expansion (*e.g.* such as for a low TCE substrate 16 and a relatively high TCE system board 82).

In an alternate embodiment of the massively parallel interface system 78b (FIG. 27) the spring probes 64a-64n on the connector 62b side of the substrate 16 mate directly to a pad matrix 88 on the test electronics modules 92a-92k.

The electrically conductive connections 64a-64n are preferably evenly distributed across the upper connector surface 62b of the substrate 16. Similarly, the conductive pads 84a-84n are preferably evenly distributed across the lower surface 139a of the system board 82. The distributed layout of the electrically conductive connections 64a-64n and the conductive pads 84a-84n provides a large connector pitch 122 and associated pad pitch 124 (*e.g.* typically on the order of 0.020-0.050 inch), whereby relatively large sized conductive pads 84a-84n and/or electrically conductive connections 64a-64n may be used. The distributed pitches 122,124 and relatively large connections promote high quality electrical connections between the substrate 16 and the system board 82 over a wide range of operating temperatures, even when the interface assembly 78a and wafer 104 are subjected to elevated temperatures, even for a substrate 16 and a system board 82 which are comprised of materials having different thermal coefficients of expansion (TCE).

The electrically conductive connections 64a-64n are connected to the system board 82, either permanently (*e.g.* such as by solder or conductive epoxy) or non-permanently (*e.g.* such as by corresponding metal pads which mate to the tips 24 of flexible spring probes 64a-64n).

In the preferred embodiment of the massively parallel interconnect assembly 78a shown in Figure 15, the plurality of electrically conductive connections 64a-64n are flexible spring probes 64a-64n. In embodiments of the substrate 16 in which the electrically conductive connections 64a-64n are flexible electrically connections 64a-64n, the flexible electrically conductive connections 64a-64n are typically fabricated using a longer spring length 28 and a larger spring angle 30b (which can be up to 360 degrees), as compared to the spring probe tips 61a-61n, to provide a compliance of approximately 4-10 mils. In some embodiments, the flexible connections 64a-64n are typically built in compliance to photolithographic springs, such as described above, or as disclosed in either U.S. Patent No. 5,848,685 or U.S. Patent No. 5,613,861, which are incorporated herein by reference.

The conductive pads 84a-84n on the lower surface of the system board 82 are typically arranged with a pad pitch 124 (FIG. 17), such that the conductive pads 84a-84n are aligned with the electrically conductive connections 64a-64n located on the upper connector surface 62b of the substrate 16.

The conductive pads 84a-84n on the lower surface of the system board 82 are then routed to conductive paths 86a-86n, which are typically arranged with a system board pitch 126. The electrically conductive connections 128a-128n, which may be arranged within one or more connection regions 132, are located on the upper surface of the system board 82, and are routed to the conductive paths 86a-86n. The electrically conductive connections 128a-128n are typically arranged in within the connection region 132, with a system board pad matrix pitch 120, which is typically aligned with the flex circuit pad matrix pitch 134 for each of the test electronics modules 92a-92k.

The system board matrix pitch 120 is typically chosen such that the electrically conductive connections 128a-128n are aligned with the flex circuit electrical connectors 119a-119n located on the flex circuits 90, which are typically arranged in a plurality of pad matrices 88 (FIG. 16), having a flex circuit pad matrix pitch 134.

The test electronics modules 92a-92k are a basic building block for most of the embodiments of the massively parallel interface test assemblies 78a-78d. The test electronics modules 92a-92k are mounted in parallel (*e.g.* as seen in Figure 15), to form an array of modules 92a-92k, which each provide electronics support to one or more columns 139 (FIG. 18, FIG. 19) on a wafer 104, or to a portion of a column 139 or die 44, along which the test electronics modules 92a-92k are mounted.

Figure 16 is a partial perspective view 110 of a massively parallel interface assembly 78a, wherein test electronics modules 92 are mounted on a frame 102. Each of the test electronics modules 92 shown includes a preferred flex circuit 90, having a pad matrix 88 of electrical contactors 119, and one or more power control modules 100. The flex circuit 90 for each of the test electronics modules 92 is mounted on one or more buss bars 98a-98h, and extends downwardly through the frame 102. The buss bars 98a-98h are attached to the frame 102, such as by electrically isolated fasteners 112, thereby providing a substantially rigid structure. The frame 102 preferably includes test module alignment guides 118, as well as frame to system alignment pins 114 and means 116 for fastening the frame 102 to a wafer chuck 106 (FIG. 15). The assembly

110 may also preferably include other means for holding the test electronics modules 92a-92k, such as a card cage (not shown) located below the frame 102.

The substrate 16 interfaces to a system board 82, which provides a standard interface to the tester electronics, at a coarser pitch. It also makes the substrate 16 a basic replacement unit, such that only the substrate 16 is typically required to be changed for a new device under test (DUT) design 44, or if the spring probes 61 need to be replaced. The combined use of standard pitch system boards 82, with substrates 16 having fanout traces 60 to small pitch spring probes 61a-61n reduces both the cost and turnaround time for test and burn-in assemblies 78.

The system board 82, which is typically comprised of ceramic, high density printed wiring board, or glass board, provides a an alignment surface for the substrate 16. Due to the larger pitch 122,124 (FIG. 17) of the connection between the system board 82 and the substrate 16, this reference can typically be achieved by mechanical means. As well, the system board 82 provides the first level routing interface between the tester electronics modules 92a-92k and the substrate 16. Each of the tester electronics modules 92a-92n are attached to the system board 82, via a membrane or flex circuit 90.

In the interface assembly 78a shown in Figure 15, the probe tips 61a-61n are flexible, which inherently provides planarity compliance between the substrate 16 and the semiconductor wafer 104. As well, the electrically conductive connections 64a-64n, which are also preferably flexible conductive springs 14, 34, 50, provide further planarity compliance between the substrate 16 and the semiconductor wafer 104. The interface assembly 78a therefore provides planarity compliance between a substrate 16 and a wafer 104. As well, the interface assembly 78a also accommodates differences in thermal coefficients of expansion (TCE) between the substrate 16 (which is typically comprised of ceramic, ceramic glass, glass, or silicon) and the system board 82 (which is typically comprised of glass epoxy material).

The flexible connections 64a-64n are preferably laid out on a standardized layout pattern, which can match standardized power and ground pad patterns (*i.e.* assignments) on the system board 82, thus allowing the same system board 82 to be used for substrates 16 laid out to mate to different integrated circuit devices

44. As a system board 82 may be adapted to specialized substrates 16, for the testing of a variety of different devices 44, the operating cost for a system board 82 is reduced.

Lower substrate standoffs 75, which are typically taller than other features on the substrate 16 (except for the spring tips 61a-61n), are preferably placed on the lower surface 62a of the substrate 16, preferably to coincide with the saw streets 94 on a semiconductor wafer under test 104, thereby preventing the wafer under test 104 from crashing into the substrate 16, and preventing damage to active regions on the semiconductor wafer 104.

Contact between test electronics modules 92a-92k and the system board 82 are achieved using solder, pressure contact, or spring probes 119,128. The spring probe tips 119,128 (FIG. 17) may have a variety of tip geometries, such as single point springs 14, interleaved springs 34, or shoulder point springs 50, and are fabricated on the substrate 16, typically using thin-film or MEMS processing methods, to achieve low manufacturing cost, well controlled uniformity, very fine pad pitches 20, and large pin counts. In some embodiments, the flexible connections 119,128 are built in compliance to photolithographic springs, such as described above, or as disclosed in either U.S. Patent No. 5,848,685 or U.S. Patent No. 5,613,861, which are incorporated herein by reference.

The configuration shown in Figure 15 brings power through the switchable power modules 100, and input/output signals 148 (FIG. 22, FIG. 23) from the pin electronics card 94 to the system board 82. This configuration has the advantage of reducing routing congestion in the flex circuit or membrane 90.

The structure of the interface assembly 78a provides very short electrical distances between the probe tips 61a-61n and the controlled impedance environment in the system board 82, which allows the interface assembly 78a to be used for high frequency applications. For embodiments wherein the traces on one or both surfaces 62a,62b of the substrate 16 are required to be impedance controlled, one or more conductive reference planes may be added within the substrate 16, either on top of the traces, below the traces, or both above and below the traces. For ultra high-frequency applications, the substrate 16 may contain alternating ground reference traces, which are connected to the one or two

reference planes 58a, 58b (FIG. 13) at regular intervals using vias 65a,65b (FIG. 13), to effectively provide a shielded coaxial transmission line environment 63.

Figure 18 is an expanded layer plan view of a wafer 104, a circular substrate 16, and a rectangular system board 82. For substrates 16 which are preferably comprised of silicon (which may be preferably chosen to match the thermal coefficient of expansion (TCE) of a wafer 104), the silicon substrate 16 may preferably be fabricated by a similar process to that of a wafer 104, such that the substrate 16 may be fabricated from a circular wafer substrate 16.

Figure 19 is an expanded layer plan view of a wafer 104, a plurality of rectangular substrates 16a, 16b, 16c and 16d, and a rectangular system board 82. For substrates which are preferably comprised of ceramic materials, the silicon substrate 16 may preferably be fabricated from one or more rectangular ceramic substrates 16a, 16b, 16c and 16d. Any of the substrates 16, 16a-16b may include a travel limit mechanism, such as one or more upper standoffs 133 located on the connector surface of the substrate 16, such as to limit perpendicular travel of the substrate in relation to the system board 82.

As seen in Figure 18 and Figure 19, devices 44, each having a plurality of pads 47, are formed on a wafer 104, and are typically populated across the wafer 104 by a series of rows 137 and columns 139, wherein saw streets are located between the rows 137 and columns 139. As can be seen in the system board 82 in Figure 18 and Figure 19, the electrically conductive connections 128a-128n, which are located on the upper surface of the system board 82, are typically arranged within one or more connection regions 132, to connect to flex circuit contactors 119 (FIG. 17), which are preferably arranged within a similar number of one or more pad matrices 88 (FIG. 16).

In some preferred embodiments of the massively parallel interface assembly 78, each of the test electronics modules 92 (*e.g.* 92a) is identical to the other test electronics modules (*e.g.* 92b-92k), thereby having an identical number of test componentry (thereby having an identical test capacity). In some embodiments of the massively parallel interface assembly 78, a similar number of devices 44 is routed to each test electronics modules 92a-92k.

In alternate embodiments of the massively parallel interface assembly 78, a different number of devices 44 may routed to a test electronics module 92 (*e.g.* 92a), such as for outer columns 139 of devices under test 44 on a specific wafer 106. For a plurality of standardized test electronics modules 92a-92k having an identical number of test componentry, a test electronics module 92 which has a greater capacity than the number of devices 44 which are connected may still be used, typically through programming the test electronics module 92 to bypass testing for unused test circuitry 94, or through system control 230.

Figure 20 is a partial cross-sectional view of one embodiment of the flexible circuit structure 142a, having a polyamide layer 144a, and opposing conductive layers 146a and 146b. Figure 21 is a partial cross-sectional view of an alternate embodiment of the flexible circuit 90, which comprises a dielectric flex circuit membrane structure 142b, and opposing conductive layers 146a and 146b. In some embodiments of the flex circuit 90, the flex circuit membrane structure 142 is inherently flexible. In alternate embodiments of the flex circuit 90, the flex circuit structure 142 is rigid in regions where one or both conductive layers are substantially located. The controlled removal of the conductive layers 146a,146b produces controlled flexibility for the flex circuit 90, while providing regions of formed conductive paths.

Figure 22 is a partial perspective view of a flexible membrane circuit structure, wherein a flexible region 90a is defined on the test card structure 94a. Figure 23 is a partial perspective view of an alternate flexible circuit structure, wherein a flexible circuit 90b is attached to a test card structure 94b by attachments 150 (*e.g.* such as but not limited to fasteners, heat staking, microwelding, or adhesives).

The test electronics 94a,94b populated on each of the test electronics modules 92a-92k provide stimulus and response detection for one or more devices under test 44. The test electronics 94a,94b are built on a high density interconnect (HDI) substrate 142a,142b, or on a standard printed wiring board 94a, which is connected to the flexible circuit 90. The test electronic card 94a,94b is populated with control and response electronics (*e.g.* such as test electronics 240 in FIG. 35). Each test electronics module 92 (*e.g.* 92a) is connected to the backend electronics and computer interface links 96 (*e.g.* typically by parallel or serial links). Alternatively, the signal pins in the tester electronics modules 92a-92k can be

connected serially, on a daisy chain, to simplify the electrical connections, such as to external test hardware. Test vector and setup information is sent to the pin electronics, from a system computer 202 and control electronics (*e.g.* such as external pattern generator 246 in FIG. 35), through the links 96.

Within each of the test electronics modules 92a-92k, a test electronics card 94, is connected to the flex circuit/membrane 90. Test electronics cards 94 may preferably be fabricated as an integral structure with the flexible circuit 90, such as on an etched thin film substrate, whereby portions of the substrate are etched, to create the flexible membrane circuit 90. In an alternate embodiment of the test electronics module, a separate test electronics card substrate 94 is connected to a flex circuit, typically by solder, wire bond or connectors.

Figure 24 is a partial cross-sectional view of one embodiment of the flex circuit region 90 of a test electronic module 92, which preferably includes a thermally conductive pathway 154 across a flex circuit 90 between a power control module 100 and one or more buss bars 98. Each of the buss bars 98a-98h, which are typically separately electrically connected to a plurality of external power supplies 234a-234h (FIG. 35), are typically electrically isolated from each other by insulators 152. The insulators 152 may be a separate layer from the buss bars 98a-98h, or may alternately be an electrically insulative layer 152 on the buss bars 98a-98h.

Figure 25 is a partial cross-sectional view of an alternate embodiment of the flex circuit region 90 of a test electronic module 92, in which one or more power control modules 100a-100h are mounted on the inner surface of the flex circuit 90, and are positioned in thermal contact with a plurality of buss bars 98a-98h.

Figure 26 is a partial cross-sectional view of a second alternate embodiment of the flex circuit region 90 of a test electronic module 92, in which a power control module 100 is electrically connected to the outer surface of a flex circuit 100. A power control access region 158 is preferably defined through the flex circuit region 90, whereby the power control module 100 positioned in intimate thermal contact with a buss bar 98 (*e.g.* such as buss bar 98b).

One or more power and ground bus bars 98a-98h are used to distribute power to all the devices under test 44. Power control modules 100, typically comprising

de-coupling capacitors, switching control circuits and regulators for each device under test 44, are preferably mounted on the flex circuit 90 as shown in Figure 24, Figure 25, or Figure 26.

While some preferred embodiments of the test electronics modules 92a-92k include flex circuit structures 90, the unique interface structure provided by the flex circuit structure 90 may alternately be achieved by other suitable interface designs. Figure 27 is a perspective view of one alternate embodiment of a test electronics module 92, in which an integrated module base 157 provides a pad matrix 88 of electrical contacts 119 on a pad matrix planar region 158. One or more power control modules 100 are electrically connected to electrical contacts 119 located the pad matrix, through power control module (PCM) traces 149, and to one or more buss bars 98a-98h. The power control modules 100 are also preferably positioned in thermal contact with one or more buss bars 98a-98h. Signal traces 148 are also connected to electrical contacts 119 located the pad matrix 88. The signal traces 148 extend across a link and component planar region 159, and are either connected to test electronics 94, or extend to link 96.

In the various embodiments of the test electronics modules 92, one or more bus bars 98 provide the power and heat sink paths for the power control modules 100. Power for devices under test 44 is typically provided through separate rail buss bars 98, or may alternately share the same rail buss bars 98 with the power control modules 100. The power rail buss bars 98 also preferably provide mechanical support for the flex circuit 90 and the system board 82 and/ or the test electronics cards 94a-94k. In some embodiments of the test electronics modules 92a-92k, the power control module circuits 100 are connected in the serial scan path, to provide individual power and ground control to the devices under test 44.

Alternate Massively Parallel Test Assemblies. Figure 28 is a partial cutaway assembly view of an alternate massively parallel test assembly 78b having an intermediate system board 82, in which flexible spring probes 160 are located on the lower surface 139b (FIG. 17) of the system board 82. The structure and features of the massively parallel test assembly 78b are otherwise identical to the massively parallel test assembly 78a shown in Figure 15. The system board spring probes 160, in conjunction with the electrically conductive connections 64a-64n on the substrate 16, provide planarity compliance between

the system board 82 and the substrate 16, and provide high quality electrical connections, over a wide range of temperatures.

Figure 29 is a partial cross-sectional view of an alternate interface assembly 78c, wherein a large grid array (LGA) interposer connector 162 is located between the substrate 16 and the system board 82. The LGA interposer connector 162 provides a plurality of conductors 164a-164n between the electrical connections 64a-64n on the substrate 16 and plurality of conductive pads 84a-84n on the lower surface of the system board 82. In one embodiment, the LGA interposer connector 162 is an AMPIFLEX™ connector, manufactured by AMP, Inc., of Harrisburg PA. In another embodiment, the interposer connector 162 is a GOREMATE™ connector, manufactured by W.L. Gore and Associates, Inc., of Eau Clare, WI. In another alternate embodiment, a pogo pin interposer 162 is used to connect opposing conductive pads 84a-84n on the system board 82 to electrical connections 64a-64n on the substrate 16.

Figure 30 is a partial cutaway assembly view of a basic massively parallel test assembly 78d, in which a substrate 16 having spring probes 61a-61n is directly connected to the test electronics modules 92a-92k. Figure 31 is a partial expanded cross-sectional view 166 of the basic massively parallel test assembly 78d, which shows staged pitch and distribution across a substrate 16 and a test electronics module 92 having a pad matrix 88 of electrical contactors 119.

Figure 32 is a partial cross sectional view 170 of an alternate massively parallel interface assembly 178e, which shows one embodiment of a basic clamping structure 172. The interface assembly 178e is typically intended for burn-in testing only, whereby test electronics 94 are packaged in small modules 174. The modules 174 are mounted directly onto the system board 82, and are preferably used for burn-in testing, which typically requires significantly less test electronics than the test electronics modules 92a-92k (*e.g.* such as shown in FIG. 15). The clamping structure 172 shown in Figure 32 may also be used for the wafer level massively parallel interface assemblies 178a-178d.

The interposer substrate 16 is preferably fabricated from a thin substrate 16, such as a 10 mil thick glass plate, whereby the substrate 16 may flex slightly, to

conform to the surface of a wafer under test, to accommodate for non-planarity or bowing between the wafer 134 and the interposer substrate 16.

A seal 180 around the periphery of the interposer substrate 16 preferably provides an air-tight chamber 182. Air pressure is preferably applied between the system board 82 and the interposer substrate 16. An applied pressure 184 also thermally isolates the DUT wafer 104 from the test electronics 174,94. While DUT wafers 104 are typically required to operate at elevated temperatures during burn-in testing (*e.g.* such as at 125-160 degrees Celsius), the test electronics 94 should preferably operate at a lower temperature (*e.g.* such as below 75 degrees Celsius).

The wafer chuck 106 preferably includes a wafer thermal control system 192, which preferably comprises a wafer heating system 194 and/or a wafer cooling system 196, such as to provide temperature control to the wafer under test 104. The wafer thermal control system 192 is preferably controlled by a test system temperature controller 188, which is typically linked 189 to the system controller 232 (FIG. 35).

The test electronics 174,94 are preferably located in one or more cooling chambers 176. A cooling system 190 is preferably used to control the operating temperature of the test electronics 174,94 within the cooling chambers 176, and is also preferably controlled by the test system temperature controller 188.

A wafer loading vacuum circuit 186, having vacuum tracks 208 (FIG. 33), is preferably built into the wafer chuck 106, to provide vacuum suction to hold the wafer under test (DUT) 104 in position, and to improve planarity between the substrate connector 16 and the wafer under test 104.

Test System Architecture. The test system consists of an alignment set up, which performs wafer alignment, cooling unit, and tester electronics. The alignment subsystem and cooling units can be built with technology known in the art.

System Alignment. Figure 33 is a first partial expanded cross-sectional view showing massively parallel test assembly 200 and alignment hardware and procedures. The test assembly 200 includes a carrier ring 202, which preferably

includes one or more alignment features, such as alignment pins 206, whereby the carrier ring 202 may be aligned to a system board 82. The system board 82 preferably has mating alignment features, such as alignment holes 226 (FIG. 34).

A substrate 16 is releaseably mounted to a carrier ring 202, such as by a flexible tape 204 (*e.g.* such as a ring-shaped KAPTON™ tape), whereby the electrical connections 64a-64n (*e.g.* such as seen in Figure 31) on the connector surface 62b of the substrate 16 are aligned to the alignment pins 206, such that the electrical connections 64a-64n on the connector surface 62b of the substrate 16 may be aligned to the conductive pads 84a-84n (FIG. 17) on the lower surface of the system board 82.

The wafer chuck 106 preferably includes a wafer loading vacuum circuit 186, having one or more wafer loading holes 208 on a wafer loading surface 209. The wafer loading vacuum circuit 186 is connectable to a vacuum source 210, and may be sealed by wafer loading vacuum circuit valve 212. A wafer to be tested 104 is placed onto the wafer chuck 106, and is held in place by a applied vacuum applied through the wafer loading holes 208.

A substrate 16, mounted on a carrier ring 202, which is to be mounted to the wafer chuck 106, is controllably positioned over the wafer 104, which is held in place by vacuum applied to the wafer chuck 106. The substrate 16 and the wafer to be tested 104 are then accurately aligned, such as by a lookup/lookdown camera 214 within a modified wafer probe system 216, whereby the probe springs 61a-61n on the probe surface 62a (FIG. 17) of the substrate 16 are brought into alignment with the die pads 47 on the DUT wafer 104. Alignment is typically achieved, either by looking at spring tips 24 (FIG. 2), or at alignment marks 77 (FIG. 14) printed on the substrate 16.

The wafer chuck 106 also preferably includes a carrier ring vacuum circuit 218, having one or more carrier ring vacuum holes 220. The carrier ring vacuum circuit 218 is also connectable to a vacuum source 210, and may be sealed by carrier ring vacuum circuit valve 222. Once the substrate 16 and the wafer to be tested 104 are accurately aligned, the lookup/lookdown camera 214 is removed, and the carrier ring 202 is controllably moved onto the wafer chuck 104, whereby the substrate 16 is accurately positioned over the wafer 16, such that the probe springs 61a-61n on the probe surface 62a of the substrate 16 contact the die

pads 47 on the DUT wafer 104. The carrier ring 202 is held in place by a vacuum applied through the carrier ring vacuum holes 220.

The wafer loading vacuum circuit valve 212 and the carrier ring vacuum circuit valve 222 are then closed, such that the applied vacuum to the wafer loading vacuum circuit 206 and the carrier ring vacuum circuit 218 is maintained, while the entire test assembly can be handled as a unit, for mounting to the system board 82 and test electronics modules 92a-92k. In alternate embodiments of the wafer loading vacuum circuit 206 and the carrier ring vacuum circuit 218, a single valve is used to apply a sealable vacuum to both vacuum circuits 206,218. To enhance the vacuum sustaining ability after the vacuum circuit valves 212 and 222 are closed, each circuit 206,218 preferably includes a vacuum chamber, which serves to maintain the vacuum level over time.

Figure 34 is a second partial expanded cross-sectional view showing massively parallel test assembly and alignment hardware and procedures 224, whereby a massively parallel interface test assembly 78 may be assembled into a system which may then be used for wafer testing. As described above, the system board 82 preferably includes a means for alignment 226 to the carrier ring and/or to the wafer chuck 106, such as alignment holes 226. The system board 82, which is mounted to the test electronics modules 92a-92k and the frame 102, is then positioned over the carrier ring 202, such that the alignment pins 206 engage the alignment holes 226. A means for attachment 228 is then typically provided, such as between the frame 102 and the wafer chuck 106 or the carrier ring 202, thus completing the assembly structure.

While accurate means (*e.g.* such as optical alignment) is typically used to align the fine pitch probe springs 61a-61n to the fine pitch pads 47 on the wafer to be tested, the mechanical alignment provided between the carrier ring 202 and the system board 82 (*e.g.* such as between alignment pins 206 and holes 226) is typically sufficient for the distributed electrical connections 64a-64n and pads 84a-84n, which preferably have larger features, and preferably have coarser pitches 122,124, respectively. As well, the flex circuit pitch 134 on the pad matrix is relatively large (*e.g.* on the order of 1 mm), making alignment between the test electronics modules 92a-92k and the system card 82 relatively easy using similar conventional mechanical alignment techniques.

Tester Electronics. Figure 35 is a partial schematic block diagram of test circuitry 230 for the massively parallel interface test systems 78. The tester electronics 230 consists of but not limited to a control computer 232, a power subsystem, test electronics modules 92a-92k, DC parametric and measurement systems 236,238, and control electronics.

As seen in Figure 35, a test electronics module 92 is typically connected to a group 264 of one or more devices to be tested 44 on a wafer 104 (*e.g.* such as but not limited to a column 139 of devices under test 44).

The test electronics modules 92a-92k each provide stimulus signals 250 to the device under test (DUT) 44, monitor the responses 254, and store the device under test pass or fail information 258 within the tester memory, or transfer the device under test pass or fail information 258 to the system controller 232.

For example, in memory testing, a test electronics module 92 has all the critical functions of a memory tester. This includes the hardware pattern generator 246 to drive the memory devices under test 44 connected to the same test electronics module 92, in parallel. Response detection and fail detection circuits in the test electronics module 92 records the fail locations for each device under test 44, as needed.

The test electronics modules 92 are preferably software re-configurable and programmable, making it possible to configure the test electronics modules 92 for a specific DUT design or test function. A built-in self-test (BIST) engine can also be integrated into the test electronics modules 92, such as to provide additional test features.

Each test electronics module 92 also provides analog multiplexing functions, to route the intended DUT pin 47 to the digital test electronics in the test electronics module 92, or to one or more DC measurement subsystems 238, which perform analog measurements of the output signals 254.

Sample Test Sequence. After a wafer to be tested 104 loaded, aligned, and engaged, the system controller 232 sends a control signal to all the power control modules 100, to connect all power and ground pins 47 for a device under test (DUT) 44 to ground, except for a selected pin 47 to be tested, which is

controllably connected to the DC parametric unit 236. The power supplies 234a-234h are disconnected from the power buses 98a-98h. The power pin integrity of the selected device 44 is then determined, through the DC parametric unit 236.

The DC parametric unit 236, which is connected to the power rails 98a-98h, via relay or solid state switches 235, is then programmed, to check for power to ground shorts. The same sequence is repeated for every power pin on every device under test 44.

Similar testing is performed on the DUT input and output pins 47, through the test electronics card 94, to determine short circuits and open circuits for a selected device under test 44. An open connection for a device under test 44 is typically detected by the absence of a parasitic diode in the input and output pins 47 of the device under test 44, as is commonly practiced in the art.

Upon the completion of setup testing, the integrity of the connections and the status of each device pin 47 is determined, in regard to open or short circuits. An excessive number of measured open circuits for one or more devices under test 44 on a wafer 104 may be due to a defective wafer 104, to system setup, or to one or more defective devices under test 44.

The test circuitry 230 preferably provides diagnostic capabilities, to further diagnose faults. Shorts can be isolated from the power busses 98 and pin test electronics 94, by scanning the appropriate bit control pattern into the power control module 100 and pin test electronics module 92.

The remaining devices to be tested 44 can then be powered up, and tested in parallel. Short circuit detection and report circuitry is preferably built into each power control module 100, such that a particular device under test 44 may be disconnected, if a short circuit is developed in the device under test while the device 44 is tested. Other features, such as but not limited to transient device current testing circuitry, may preferably be included within the power control module 100, such as to provide additional test coverage.

Power Pin Testing. The system controller 232 selectively switches on the power connections to one or more devices under test 44. With the power

supplies 234a-234h turned off (disconnected), a device under test 44 can be tested for open circuits and short circuits, using the DC parametric unit 236.

I/O Pin Testing. Similarly, the input and output pins 47 on a device under test 44 can be tested for leakage, open, shorts, through the system controller 232.

Device Functional Testing. With test results from power pin testing and I/O Pin Testing, for any devices under test 44 which have failed (*e.g.* due to power), the input and output pins 47 for the failed devices 44 are typically isolated from the tester common resources. The remaining devices under test 44 which have passed power pin testing and I/O pin testing are then powered up, and may then be tested in parallel.

Functional Testing. The stimulus unit 248 and pattern generator 246 generate the input pattern 250 to the device under test 44. The DUT response 254 is captured in the response block 256, which compares the device under test 44 output with the expected value from the pattern generator 246 or stimulus unit 248. A pattern generator 246 is commonly used in memory testing, whereas a truth table representing the device stimulus 250 and expected response 254 can be stored in the pattern memory of the stimulus unit 248 for logic device testing. A fail map or log 258 is maintained for each die 44. While Figure 35 portrays one embodiment of the functional schematic of the pattern generation and stimulus/response system architecture, other pattern generation and stimulus/response system architectures may suitably be used to meet the testing requirements of a device under test 44, as is commonly practiced in the art.

Alternate Interface Embodiments. Figure 36 is a partial cutaway assembly view of a massively parallel interface assembly 270a, in which a plurality of interface modules 272a-272j are electrically connected to a system interconnect board 286a. Each of the interface modules 272 (*e.g.* such as 272a) includes a pad matrix 88 of electrical conductors 119, which are each electrically connected to a probe spring interposer 276.

Each of the probe spring interposer 276 includes lower surface spring probes 280, electrically connected to upper surface spring probes 284 by vias 282. As described above, the lower surface spring probes 280, as well as the upper

surface spring probes 284, may have a variety of tip geometries, such as single point springs 14, interleaved springs 34, or shoulder point springs 50, and are fabricated on the substrate 16, typically using thin-film or MEMS processing methods, to achieve low manufacturing cost, well controlled uniformity, very fine pad pitches 20, and large pin counts. In some embodiments, the flexible connections lower surface spring probes 280 and/or the upper surface spring probes 284 are built in compliance to photolithographic springs, such as described above, or as disclosed in either U.S. Patent No. 5,848,685 or U.S. Patent No. 5,613,861, which are incorporated herein by reference.

The probe spring interposers 276 are provide electrical connections between each of the interface modules 272a-272j and the system interconnect board 286a. The system interconnect board 286a has upper surface electrical contactors 290, vias 291, upper surface interconnection structures 292 and lower surface interconnection structures 292 294, such that one or more pads one each interface modules 272 may typically be connected together. The system interconnect board 286a may also preferably include board electrical componentry, which may be electrically connected to one or more of the interface modules 272. Each of the interface modules 272 includes links 96 which provide electrical connections to the system interconnect board 286a , and may also preferably include interface module circuitry 298.

Figure 37 is a partial cutaway assembly view of an alternate massively parallel interface assembly 270b, in which a plurality of interface modules 272a-272j are electrically connected, through a system board interposer 300 to a system interconnect board 286b, which includes flexible probe spring 64a-64n, as described above. The system board interposer 300 may preferably include interconnection structures 302 and/or board electrical componentry 304, which may be electrically connected to one or more of the interface modules 272.

The massively parallel interface assemblies 270a,270b each provide a versatile and robust interface between a plurality of interconnected structures. The massively parallel interface assembly 270a may simply be used to provide a robust massively parallel interface (such as to provide complex parallel connections between similar components). In preferred interface embodiments, the massively parallel interface assemblies 270a,270b may also include module specific electronic circuitry 298, or shared circuitry 296.

Figure 38 is a schematic block diagram 306 of connections between a plurality of computer systems 308a-308n, using a massively parallel interface assembly 270. Figure 39 is a schematic block diagram 310 of connections between a plurality of electronic circuits 312a-312n, using a massively parallel interface assembly 270.

System Advantages. The massively parallel interface assemblies 78a-78d provide signal and power interconnections between a test system and a large number of devices 44 located on a wafer 104, while providing planarity compliance between the wafer 104 and successive assembly layers (*e.g.* such as substrate 16, system board 82, and the pad matrices 88 on the test electronics modules 92a-92k.

As well, the massively parallel interface assemblies 78a-78d provide short electrical paths for the power and input and output signals, between the test electronics modules 92a-92k and the devices under test 44, through the combined use of high pitch spring probe tips 61a-61n, layered substrates 16,82, and the vertically packaged test electronics modules 92a-92k, which typically include flex circuits 90.

Furthermore, while the massively parallel interface assemblies 78a-78d provide short electrical paths for the power and input and output signals, between the test electronics modules 92a-92k and the devices under test 44 (thereby reducing round trip transit time), the massively parallel interface assemblies 78a-78d provide thermal isolation between the test electronics 94 and the devices under test 44, while providing a uniform force across all mating spring probe 61/pad 47 pairs over the entire wafer 104, such that the devices under test 44 may be controllably operated over a wide temperature range, while the test electronics modules 92a-92k provide enhanced heat transfer away from heat sensitive components (*e.g.* such as through buss bars 98a-98h), and while preferably providing enhanced test module temperature control.

As well, while the devices under test 44 may be controllably operated over a wide temperature range, the massively parallel test interface structure 78a-78c preferably provides provide signal and power interconnections between a test system and a large number of devices 44 located on a wafer 104, which are

maintained over the temperature range, through the use of suitably sized, coarse pitch 122,124 interconnections between substrate 16 and the system board 82 (which maintains electrical contact between the coarse pitch 122,124 interconnections 64a-64n over the temperature range), and through the specified use of a substrate 16 having a similar coefficient of thermal expansion to the wafer under test 104 (which maintains electrical contact between the fine pitch 20 interconnections 61a-61n over the temperature range).

As described above, the massively parallel test interface assemblies 78 may be used to detect power to ground shorts in any die quickly, and to isolate power from a die having a detected power to ground short before damage is done to the test electronics. In addition, the massively parallel test interface assemblies 78 and related test system may be used to detect that the contacts to many, hundreds, or even hundreds of thousands of pads are reliably made and whether each of the contacts are within the contact resistance specification, and to assure that the self inductance and self capacitance of each signal line are below values that would adversely affect test signal integrity.

Furthermore, the massively parallel test interface assemblies 78 and related test system can be used to detect whether the mutual inductance and mutual capacitance between pairs of signal lines and between signal lines and power or ground lines are below values that would adversely affect test signal integrity.

As well, the massively parallel test interface assemblies 78 provide stimulus and response detection and analysis to many, hundreds, or even thousands, of die under test in parallel, and which preferably provides diagnostic tests to a failed die, in parallel with the continued testing of all other die.

In addition, the massively parallel test interface assemblies 78 can reliably and repeatedly establish contact to many, hundreds, or even hundreds of thousands of pads 47, without the need to periodically stop and inspect and/or clean the probe interface structure 16.

Furthermore, the massively parallel test interface assemblies 78 inherently organize and manage the interconnections between the devices under test 44 and the tester electronics 230, while maintaining signal integrity and power and

ground stability, and assures that no two or more adjacent pads 47 are contacted by a single test probe tip.

Although the disclosed massively parallel interface assemblies are described herein in connection with integrated circuit testing, computer networking, and circuit connections, the assemblies and techniques can be implemented with a wide variety devices and circuits, such as interconnections between integrated circuits and substrates within electronic components or devices, burn-in devices and MEMS devices, or any combination thereof, as desired.

Accordingly, although the invention has been described in detail with reference to a particular preferred embodiment, persons possessing ordinary skill in the art to which this invention pertains will appreciate that various modifications and enhancements may be made without departing from the spirit and scope of the claims that follow.

CLAIMS

What is claimed is:

1. A system for connection to at least one integrated circuit device on a wafer, comprising:

a system board having a bottom surface and a top surface, and a plurality of electrical conductors extending between said bottom surface and said top surface;

a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips for connection to said at least one integrated circuit device, and a plurality of electrical connections extending through said substrate between each of said plurality of said spring probe contact tips and said connector surface;

a plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board;

at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of said electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of said at least one interconnection region; and

means for fixedly holding each of said at least one interface module in relation to said system board, such that said plurality of electrically conductive pads on said planar region of each of said at least one interface module contact at least one of said plurality of electrical conductors on said top surface of said system board.

2. The system of Claim 1, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographically patterned springs.

3. The system of Claim 1, wherein said plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board are flexible spring probes on said connector surface of said substrate.

4. The system of Claim 3, wherein said flexible spring probes on said connector surface of said substrate are photolithographically patterned springs.

5. The system of Claim 1, wherein said plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board are flexible spring probes on said bottom surface of said system board.

6. The system of Claim 5, wherein said flexible spring probes on said bottom surface of said system board are photolithographically patterned springs.

7. The system of Claim 1, wherein each of said at least one interface module includes a circuit having a first surface and a second surface, and wherein said plurality of electrically conductive pads are located on said first surface.

8. The system of Claim 7, wherein said circuit is a flexible circuit.

9. The system of Claim 7, wherein said circuit is a semi-rigid circuit.

10. The system of Claim 7, wherein said circuit is a rigid circuit.

11. The system of Claim 1, further comprising:

an interposer substrate located between said connector surface of said substrate and said bottom surface of said system board, wherein said plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and each of said electrical conductors on said bottom surface of said system board are located within said interposer substrate.

12. The system of Claim 1, further comprising:

at least one buss bar electrically connected to at least one of said at least one said interconnection region.

13. The system of Claim 12, further comprising:

at least one power control module located on said at least one interface module, each of said at least one power control module electrically connected

between said at least one buss bar and at least one of said at least one said interconnection region.

14. The system of Claim 13, wherein said at least one power control module is in thermal contact with said at least one buss bar.

15. The system of Claim 12, further comprising:

at least one power control module located on said at least one buss bar, each of said at least one power control module electrically connected between said at least one buss bar and at least one of said at least one said interconnection region.

16. The system of Claim 15, wherein said at least one power control module is in thermal contact with said at least one buss bar.

17. The system of Claim 1, further comprising:

at least one lower substrate standoff fixedly attached to said probe surface of said substrate.

18. The system of Claim 1, further comprising:

a travel limit mechanism which limits perpendicular travel of said substrate in relation to said system board.

19. The system of Claim 1, wherein said substrate includes a plurality of holes defined therethrough between said probe surface and said connector surface, and wherein each of said plurality of electrical connections between each of said contact tips and each of said electrically conductive connections are electrically conductive vias located within each of said plurality of holes in said substrate.

20. The system of Claim 1, wherein said substrate is electrically insulative.

21. The system of Claim 1, wherein said substrate is dielectric.

22. The system of Claim 1, wherein said substrate is electrically conductive.

23. The system of Claim 1, wherein said substrate is comprised of a material having a similar thermal coefficient of expansion to said wafer.

24. The system of Claim 1, further comprising:
an assembled component located on said substrate.

25. The system of Claim 24, wherein said assembled component is a passive component.

26. The system of Claim 25, wherein said passive assembled component is a capacitor.

27. The system of Claim 24, wherein said assembled component is an active component.

28. The system of Claim 1, further comprising:
a component incorporated as a fabricated structure of said substrate.

29. The system of Claim 28, wherein said fabricated structure is a passive component.

30. The system of Claim 29, wherein said passive fabricated structure is a capacitor.

31. The system of Claim 28, wherein said fabricated structure is an active component.

32. The system of Claim 1, wherein said substrate comprises silicon.

33. A system for connection to at least one integrated circuit device on a wafer, comprising:

a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips for connection to said at least one integrated circuit device, and a plurality of electrical connections extending through said substrate between each of said plurality of said contact tips and said connector surface;

at least one interface module having a plurality of electrically conductive pads on a planar region, at least one of said electrically conductive pads connected to at least one interconnection region, and at least one link connected to at least one of said at least said interconnection region; and

a plurality of electrically conductive connections between each of said plurality of electrical connections on said connector surface of said substrate and said plurality of electrically conductive pads located on said planar region of said at least one interface module; and

means for fixedly holding each of said at least one interface module in relation to said substrate, such that said plurality of electrically conductive pads on said planar region of each of said at least one interface module contact at least one of said plurality of electrical connections on said connector surface of said substrate.

34. The system of Claim 33, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographic springs.

35. The system of Claim 33, wherein said plurality of electrical connections on said connector surface of said substrate are flexible spring probes.

36. The system of Claim 35, wherein said flexible spring probes on said connector surface of said substrate are photolithographic springs.

37. The system of Claim 33, wherein each of said at least one interface module includes a circuit having a first surface and a second surface, and wherein said plurality of electrically conductive pads are located on said first surface.

38. The system of Claim 37, wherein said circuit is a flexible circuit.

39. The system of Claim 37, wherein said circuit is a semi-rigid circuit.

40. The system of Claim 37, wherein said circuit is a rigid circuit.

41. The system of Claim 33, further comprising:

at least one buss bar electrically connected to at least one of said at least one said interconnection region.

42. The system of Claim 41, further comprising:

at least one power control module located on said at least one interface module, each of said at least one power control module electrically connected

between said at least one buss bar and at least one of said at least one said interconnection region.

43. The system of Claim 42, wherein said at least one power control module is in thermal contact with said at least one buss bar.

44. The system of Claim 41, further comprising:

at least one power control module located on said at least one buss bar, each of said at least one power control module electrically connected between said at least one buss bar and at least one of said at least one said interconnection region.

45. The system of Claim 44, wherein said at least one power control module is in thermal contact with said at least one buss bar.

46. The system of Claim 33, further comprising:

at least one lower substrate standoff fixedly attached to said probe surface of said substrate.

47. The system of Claim 33, further comprising:

a travel limit mechanism which limits perpendicular travel of said substrate in relation to said at least one of said at least one interface module.

48. The system of Claim 33, wherein said substrate includes a plurality of holes defined therethrough between said probe surface and said connector surface, and wherein each of said plurality of electrical connections between each of said contact tips and each of said electrically conductive connections are electrically conductive vias located within each of said plurality of holes in said substrate.

49. The system of Claim 33, wherein said substrate is electrically insulative.

50. The system of Claim 33, wherein said substrate is dielectric.

51. The system of Claim 33, wherein said substrate is electrically conductive.

52. The system of Claim 33, wherein said substrate is comprised of a material having a similar thermal coefficient of expansion to said wafer.

53. The system of Claim 33, further comprising:
an assembled component located on said substrate.

54. The system of Claim 53, wherein said assembled component is a passive component.

55. The system of Claim 54, wherein said passive assembled component is a capacitor.

56. The system of Claim 53, wherein said assembled component is an active component.

57. The system of Claim 33, further comprising:
a component incorporated as a fabricated structure of said substrate.

58. The system of Claim 57, wherein said fabricated structure is a passive component.

59. The system of Claim 58, wherein said passive fabricated structure is a capacitor.

60. The system of Claim 57, wherein said fabricated structure is an active component.

61. The system of Claim 33, wherein said substrate comprises silicon.

62. An interface module, comprising:
an electrically insulative module base extending from a planar region;
a plurality of electrically conductive pads located on said planar region of said electrically insulative module base;
a power control module in contact with said electrically insulative module base, and having at least one electrical connection to one of said plurality of electrically conductive pads; and
an electrical conductor in electrical contact and in thermal contact with said power control module, a portion of said electrical conductor extending from said electrically insulative module base.

63. The interface module of Claim 62, further comprising:

a plurality of conductive traces connected to said plurality of electrically conductive pads located on said planar region and extending to a link connection.

64. The interface module of Claim 62, further comprising:

at least one electronic component located on said electrically insulative module base; and

at least one component trace connected between said least one electronic component and said link region.

65. The interface module of Claim 62, further comprising:

at least one electronic component located on said electrically insulative module base; and

at least one component trace connected between said least one electronic component and at least one of said plurality of electrically conductive pads located on said planar region.

66. The interface module of Claim 62, further comprising:

at least one electronic component located on said electrically insulative module base; and

at least one component trace connected between said least one electronic component and at least one of said plurality of electrically conductive pads located on said planar region.

67. The interface module of Claim 62, further comprising:

a plurality of spring probes connected to said plurality of electrically conductive pads and extending from said planar region of said electrically insulative module base.

68. The interface module of Claim 67, wherein said plurality of spring probes are photolithographically patterned springs.

69. A process, comprising the steps of:

providing a substrate having a probe surface and a connector surface, said probe surface having a plurality of spring probe contact tips, and a plurality of

electrical connections extending through said substrate between each of said plurality of said contact tips and said connector surface;

providing a wafer having a lower surface and an upper surface, and having a plurality of pads located on said upper surface;

attaching said wafer to a wafer carrier;

providing a carrier ring having a hollow portion defined therethrough;

attaching said substrate to said carrier ring, such that said substrate is generally located within said hollow portion of said carrier;

bringing said attached substrate and said attached wafer into alignment, such that said plurality of spring probe contact tips on said probe surface of said attached substrate are in alignment to said plurality of pads located on said upper surface of said wafer; and

moving said carrier ring and said wafer carrier into contact, such that said aligned plurality of spring probe contact tips on said probe surface of said attached substrate contact said aligned plurality of pads located on said upper surface of said wafer.

70. The process of Claim 69, wherein said step of attaching said wafer to said wafer carrier includes aligning said wafer to said wafer carrier.

71. The process of Claim 69, wherein said step of attaching said substrate to said carrier ring includes aligning said substrate to said carrier ring.

72. The process of Claim 69, wherein said alignment between said attached substrate and said attached wafer is an optical alignment.

73. The process of Claim 69, wherein said plurality of spring probe contact tips on said probe surface of said substrate are photolithographically patterned springs.

74. The process of Claim 69, wherein said plurality of electrical connections which extend to said connector surface on said substrate include flexible spring probes on said connector surface of said substrate.

75. The process of Claim 74, wherein said flexible spring probes on said connector surface of said substrate are photolithographically patterned springs.

76. The process of Claim 69, further comprising the step of:
attaching said carrier ring to said wafer carrier.

77. The process of Claim 69, further comprising the steps of:
proving a test structure having a bottom surface, and a plurality of electrical conductors located on said bottom surface;
bringing said test structure and said carrier ring into alignment, such that said plurality of electrical conductors located on said bottom surface of said test structure are in alignment to said plurality of electrical connections on said connector surface of said substrate; and
moving said aligned test structure and said carrier ring, such that said aligned plurality of electrical conductors located on said bottom surface of said test structure contact said aligned plurality of electrical connections on said connector surface of said substrate.

78. The process of Claim 77, wherein said alignment between said test structure and said carrier ring is a mechanical alignment.

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(74) Agents: **GLENN, Michael, A.** et al.; Glenn Patent Group, 3475 Edison Way, Ste. L, Menlo Park, CA 94025 (US).

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Published:
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MASSIVELY PARALLEL INTERFACE FOR ELECTRONIC CIRCUIT

(57) Abstract: Several embodiments of massively parallel interface structures are disclosed, which may be used in a wide variety of permanent or temporary applications, such as for interconnecting integrated circuits (ICs) to test and burn-in equipment, for interconnecting modules within electronic devices, for interconnecting computers and other peripheral devices within a network, or for interconnecting other electronic circuitry. Preferred embodiments of the massively parallel interface structures provide massively parallel integrated circuit test assemblies. The massively parallel interface structures preferably use one or more substrates to establish connections between one or more integrated circuits on a semiconductor wafer, and one or more test modules. One or more layers on the intermediate substrates preferably include MEMS and/or thin-film fabricated spring probes. The parallel interface assemblies provide tight signal pad pitch and compliance, and preferably enable the parallel testing or burn-in of multiple ICs, using commercial wafer probing equipment. In some preferred embodiments, the parallel interface assembly structures include separable standard electrical connector components, which reduces assembly manufacturing cost and manufacturing time. These structures and assemblies enable high speed testing in wafer form.

WO 00/73905 A2

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8

Fig. 9

Fig. 11

Fig. 10

Fig. 12

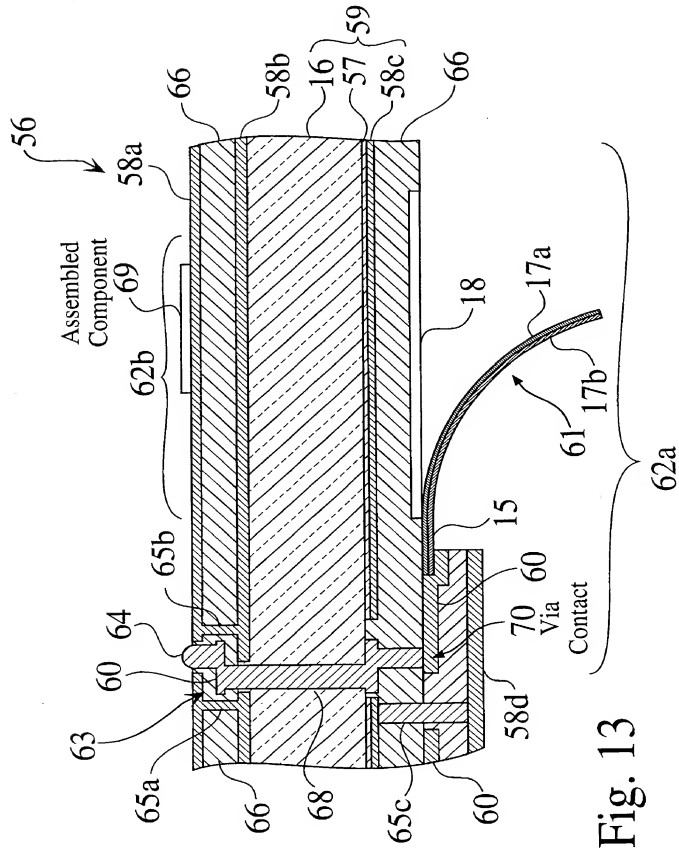

56
58a
66
58b
16
57
58c
59
66
Assembled Component
69
62b
18
17a
17b
61
62a
65b
15
64
60
63
65a
66
68
65c
60
58d
70
Via Contact
60

Fig. 13

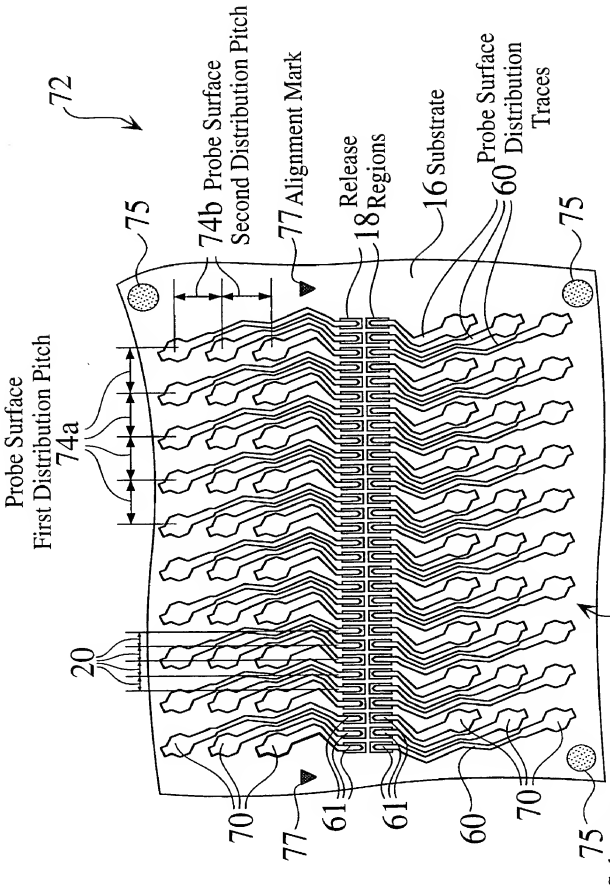

72
Probe Surface
First Distribution Pitch
74a
74b Probe Surface
Second Distribution Pitch
77 Alignment Mark
Release
18 Regions
16 Substrate
Probe Surface
60 Distribution
Traces
75
20
62a
70
77
61
61
60
70
75
Substrate
Standoff

Fig. 14

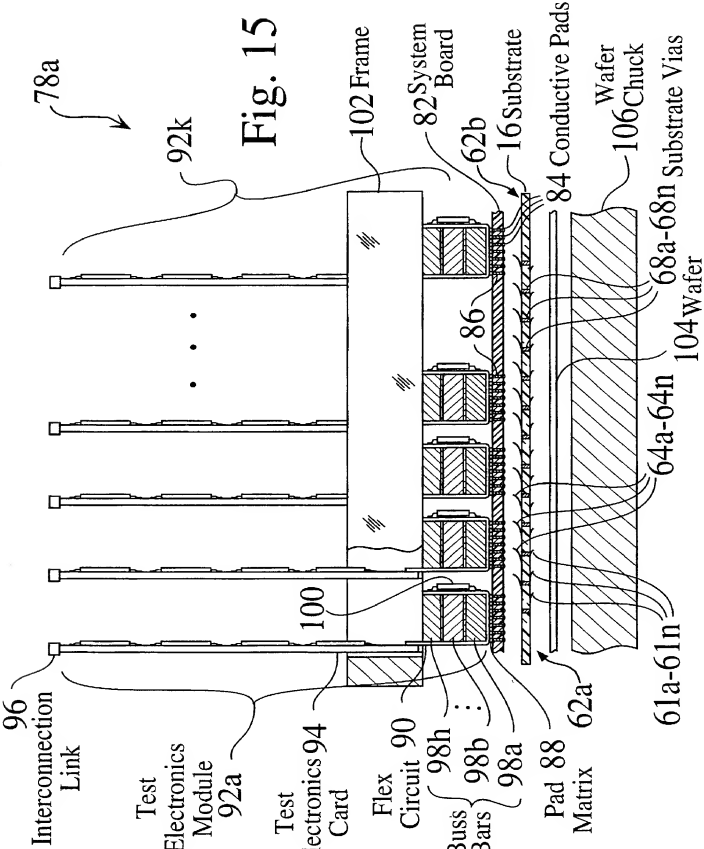

78a
92k
102 Frame
82 System Board
62b
16 Substrate
84 Conductive Pads
Wafer Chuck 106
Substrate Vias
68a-68n
86
104 Wafer
64a-64n
61a-61n
62a
100
96 Interconnection Link
Test Electronics Module 92a
Test Electronics Card 94
Flex Circuit 90
98h
98b
98a
Buss Bars
Pad Matrix 88

Fig. 15

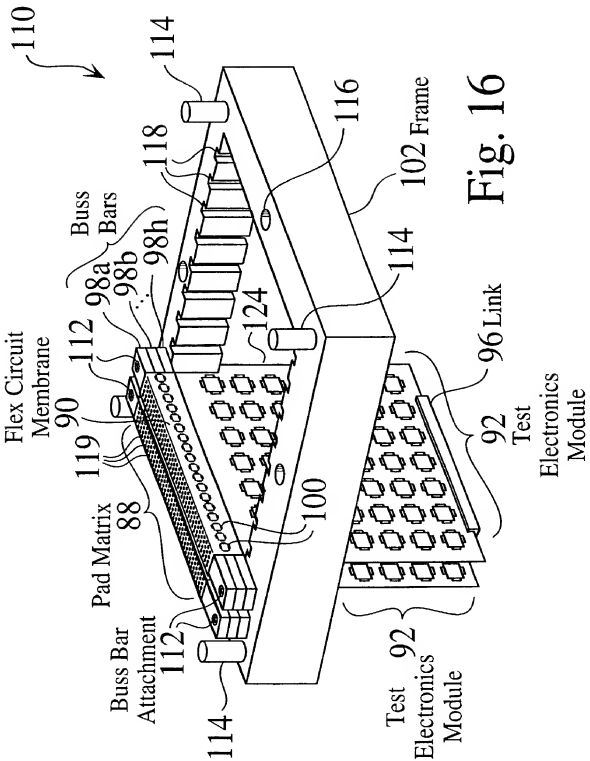
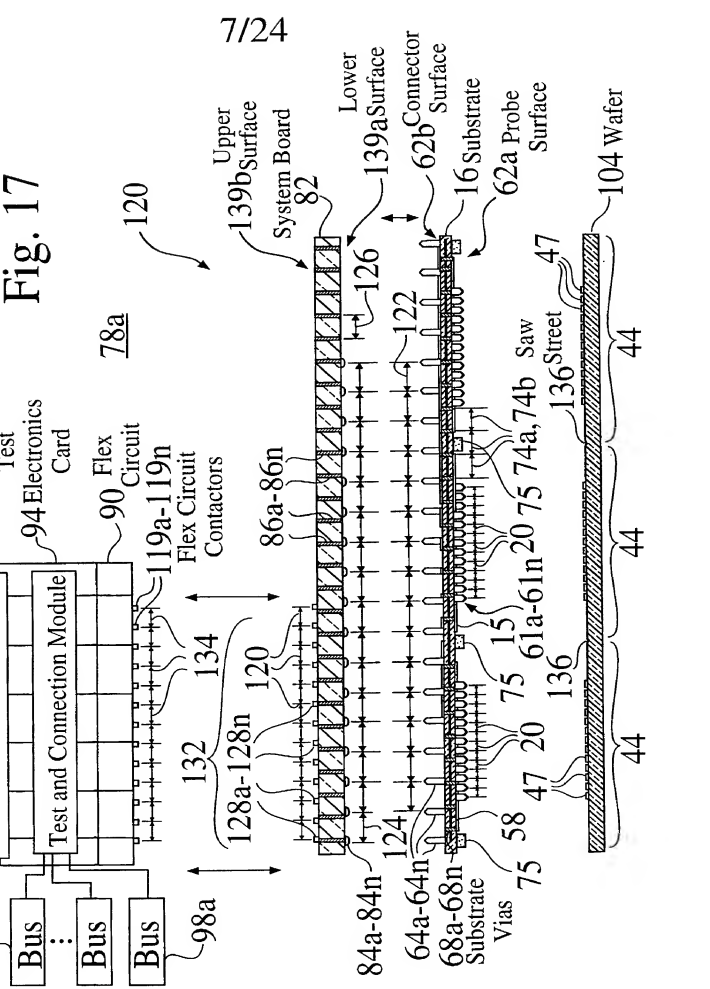

110
114
118
Buss Bars
98a
98b
98h
116
102 Frame
112
124
114
Flex Circuit Membrane
90
119
96 Link
Pad Matrix
88
100
92 Test Electronics Module
Buss Bar Attachment
112
114
92 Test Electronics Module

Fig. 16

Fig. 17


92
96 Link
94 Test Electronics Card
Test and Connection Module
90 Flex Circuit
119a-119n Flex Circuit Contactors
98h
Bus
Bus
Bus
98a
78a
120
System Board 82
Upper Surface 139b
Lower Surface 139a
Connector Surface 62b
16 Substrate
Probe Surface 62a
104 Wafer
126
122
Saw Street 136
47
44
86a-86n
74a, 74b
75
20
15
61a-61n
134
132
120
128a-128n
124
84a-84n
64a-64n
68a-68n
Substrate Vias
58

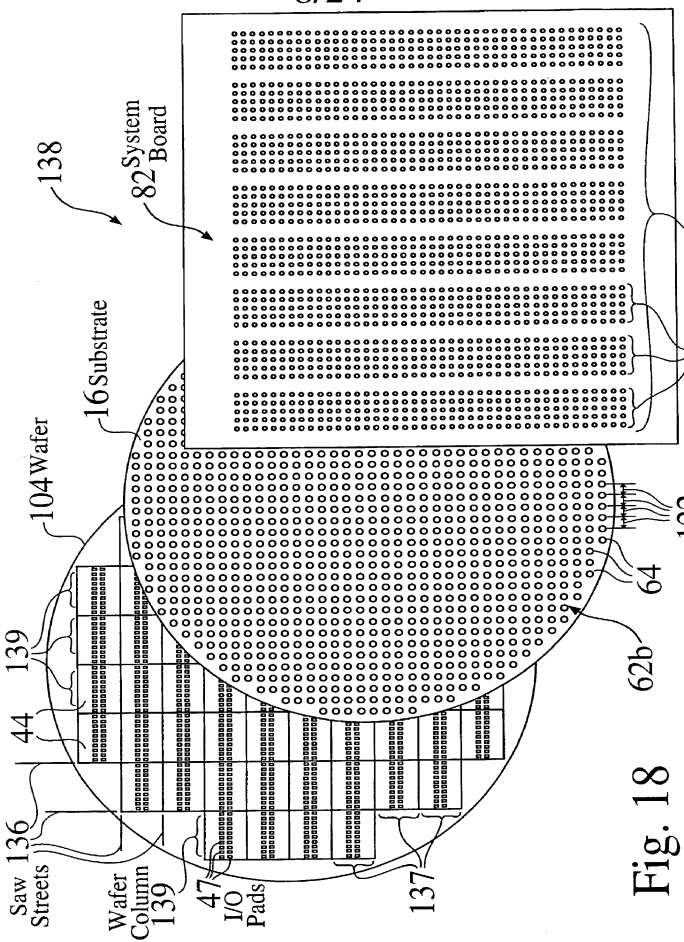

138
82 System Board
16 Substrate
104 Wafer
139
44
136
Saw Streets
Wafer Column 139
47
I/O Pads
137
62b
64
122
132
128a-128n

Fig. 18

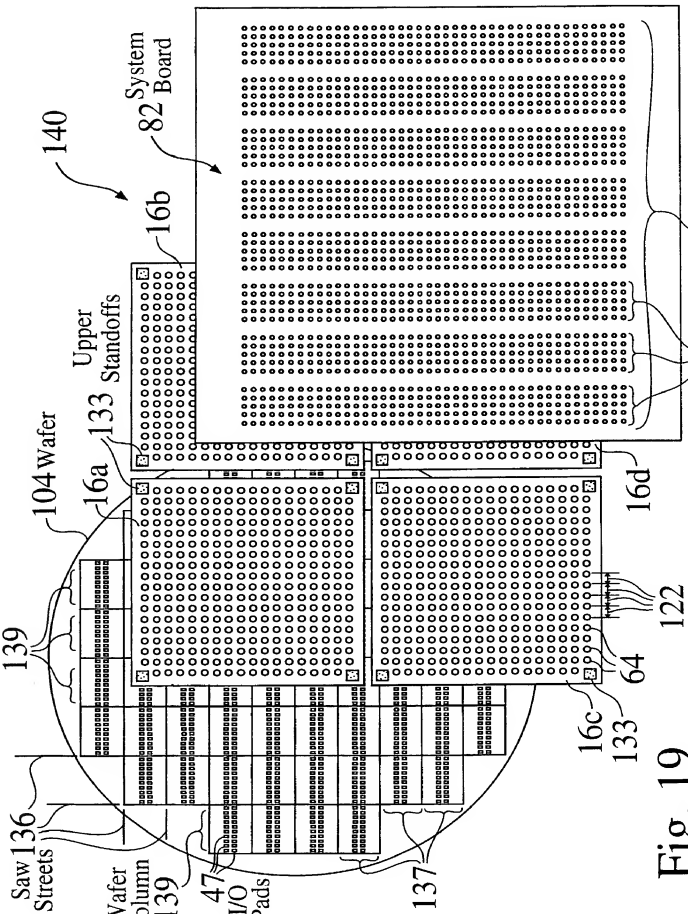

140
82 System Board
16b
Upper Standoffs
133
104 Wafer
16a
139
Saw Streets 136
Wafer Column 139
47 I/O Pads
137
16c
133
64
122
16d
132
128a-128n

Fig. 19

Fig. 20

Fig. 21

Fig. 23

Fig. 22

Fig. 26

Fig. 24

Fig. 25

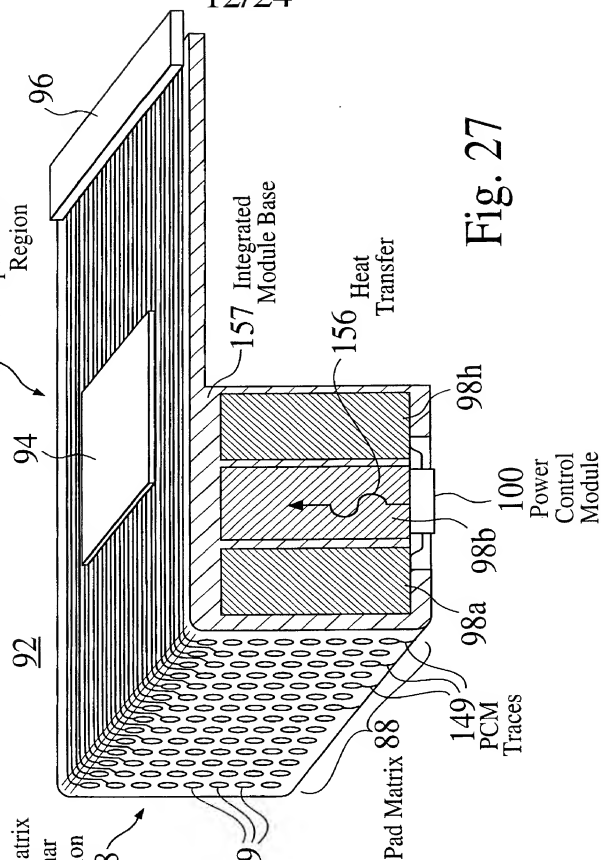

96
Link and Component Planar Region
159
94
92
Integrated Module Base
157
Heat Transfer
156
98h
100
Power Control Module
98b
98a
149
PCM Traces
Pad Matrix
88
119
Pad Matrix Planar Region
158

Fig. 27

Fig. 28

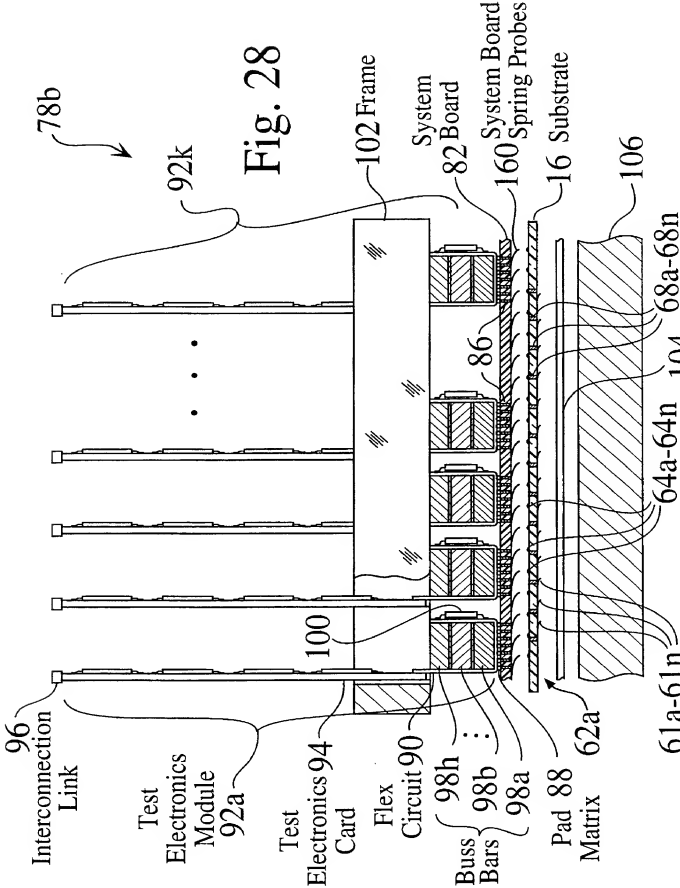

78b
92k
102 Frame
System Board 82
System Board Spring Probes 160
16 Substrate
106
68a-68n
86
104
64a-64n
100
96 Interconnection Link
Test Electronics Module 92a
Test Electronics Card 94
Flex Circuit 90
98h
98b
98a
Buss Bars
Pad Matrix 88
62a
61a-61n

Fig. 29

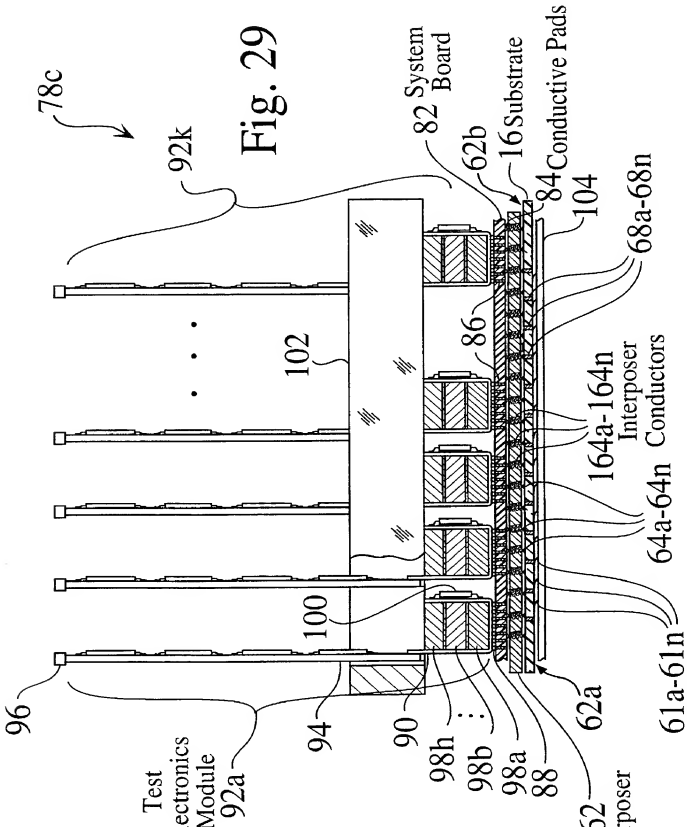

78c
92k
82 System Board
62b
16 Substrate
84 Conductive Pads
104
68a-68n
86
102
164a-164n Interposer Conductors
64a-64n
100
96
94
90
98h
98b
98a
88
62a
61a-61n
Test Electronics Module 92a
162 Interposer

Fig. 30

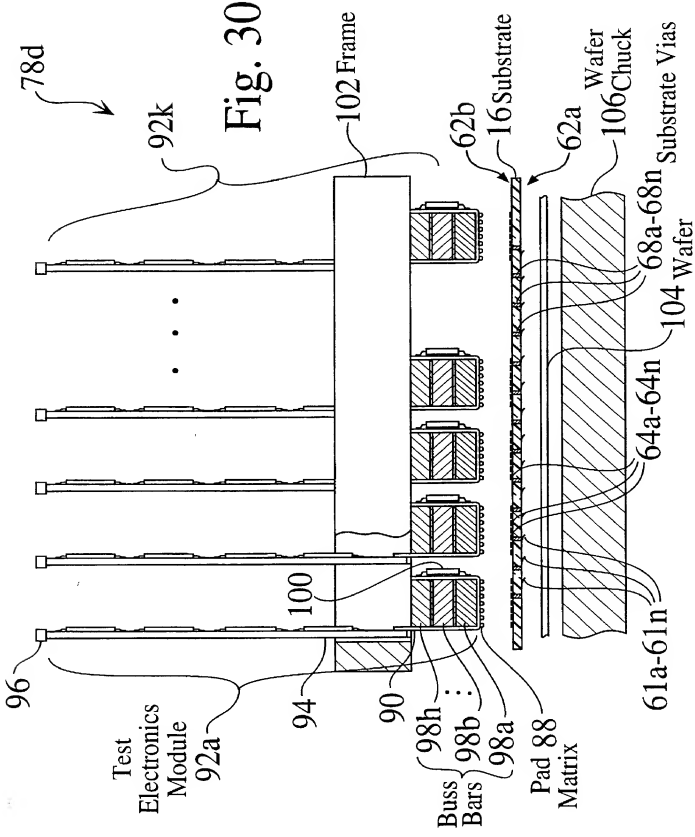

78d
92k
102 Frame
62b
16 Substrate
62a
Wafer Chuck 106
Substrate Vias
68a-68n
104 Wafer
64a-64n
61a-61n
96
Test Electronics Module 92a
94
90
100
98h
98b
98a
Buss Bars
Pad Matrix 88

Fig. 31

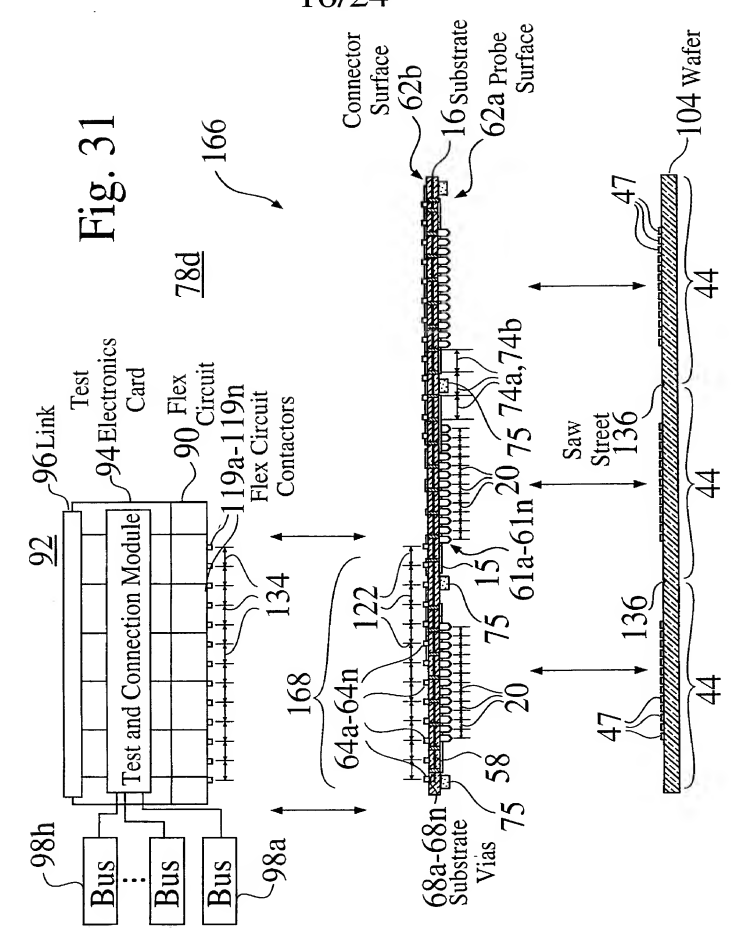
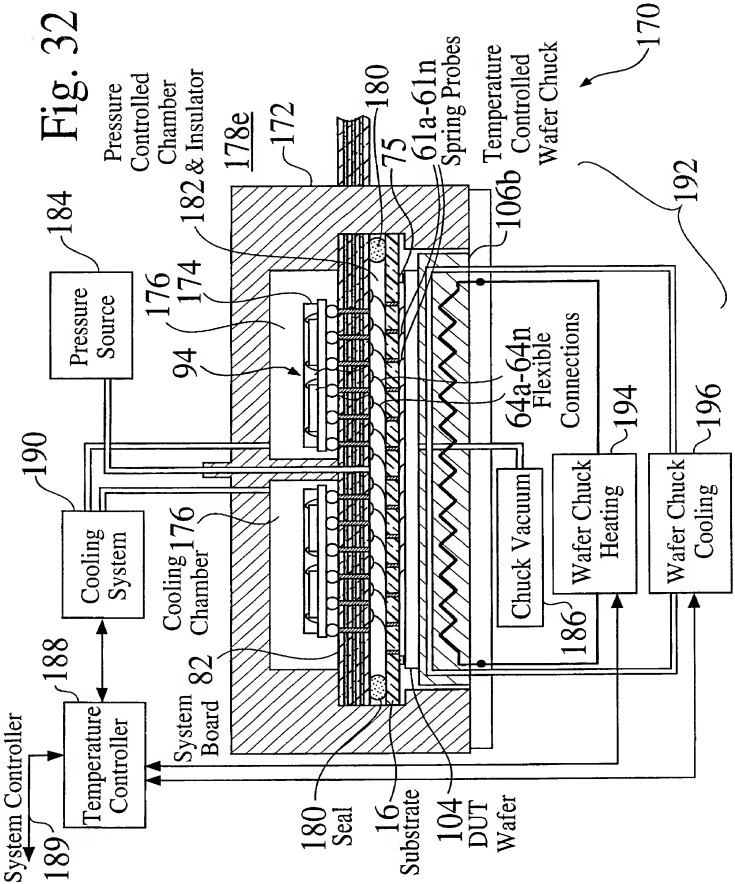

92
96 Link
Test Electronics Card
94
Test and Connection Module
90 Flex Circuit
119a-119n Flex Circuit Contactors
98h
Bus
Bus
Bus
98a
78d
166
Connector Surface
62b
16 Substrate
62a Probe Surface
104 Wafer
168
64a-64n
122
134
68a-68n Substrate Vias
58
75
20
15
61a-61n
74a,74b
Saw Street
136
47
44

Fig. 32


To System Controller
189
Temperature Controller
188
Cooling System
190
Pressure Source
184
Pressure Controlled Chamber & Insulator
178e
182
Cooling Chamber
176
System Board
82
180 Seal
16 Substrate
104 DUT Wafer
94
176
174
172
180
75
61a-61n Spring Probes
Temperature Controlled Wafer Chuck
170
106b
192
64a-64n Flexible Connections
Chuck Vacuum
186
Wafer Chuck Heating
194
Wafer Chuck Cooling
196

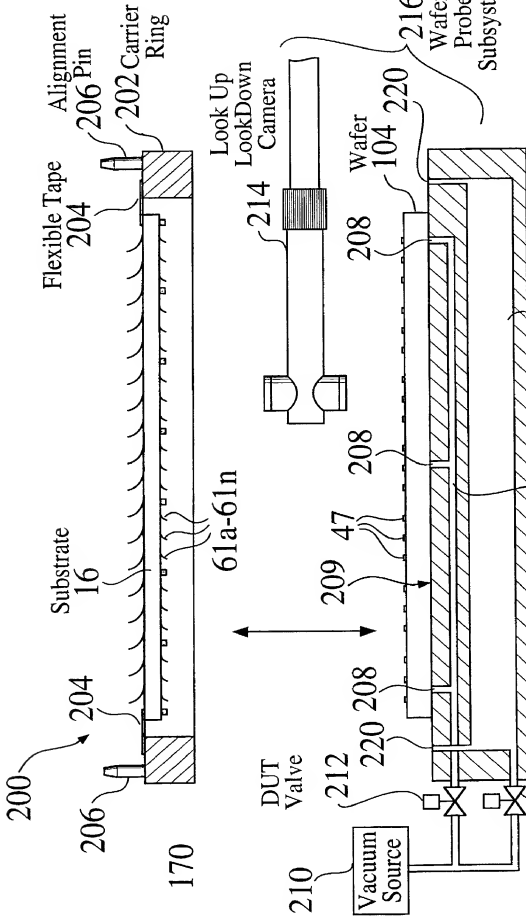

200
206
204
170
Substrate
16
Flexible Tape
204
Alignment
Pin
206
202 Carrier
Ring
61a-61n
Look Up
LookDown
Camera
214
209
47
208
208
220
DUT
Valve
212
210
Vacuum
Source
222
Carrier Ring
Valve
186
Wafer Loading
Vacuum Circuit
106
218 Carrier Ring
Vacuum Circuit
Wafer
104
220
216
Wafer
Probe
Subsystem

Fig. 33

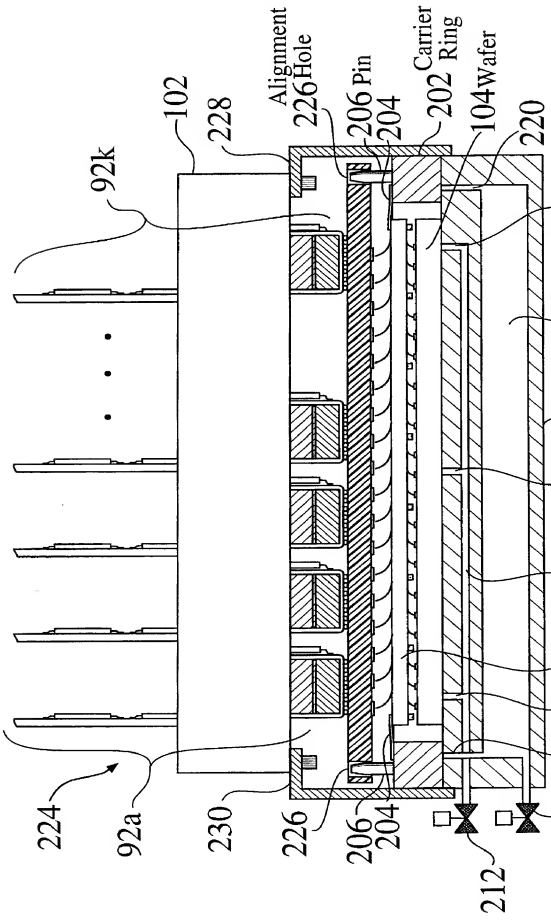

Alignment Hole
226
Pin
206
204
Carrier Ring
202
Wafer
104
220
102
228
92k
208
218
106
208
186
16
Substrate
208
220
224
92a
230
226
206
204
212
222

Fig. 34

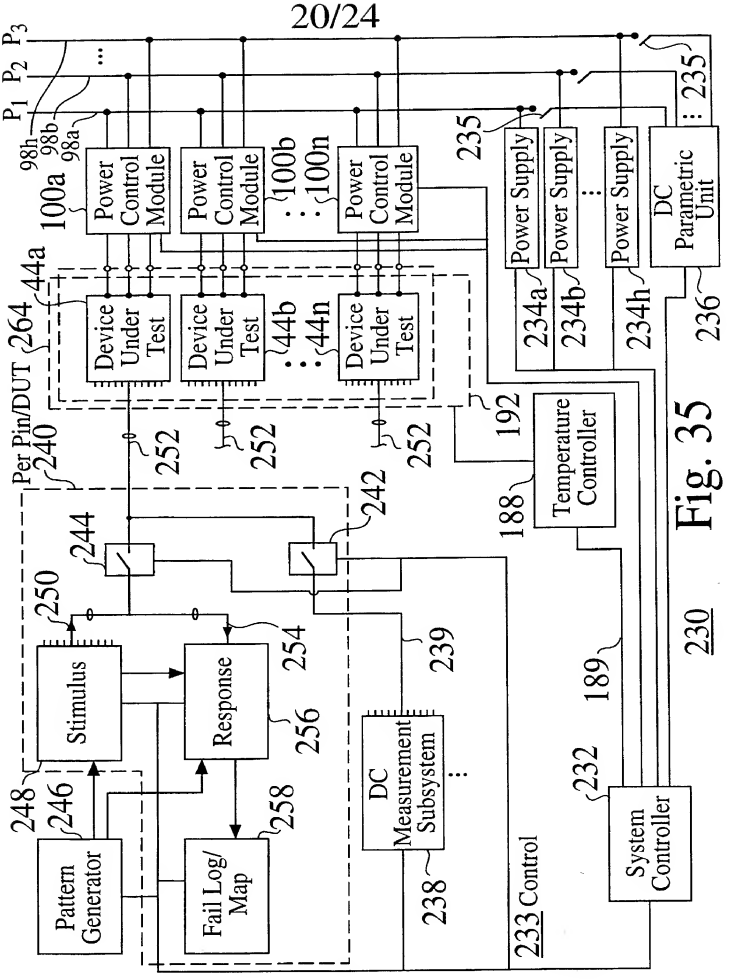

P1 P2 P3
98h 98b 98a
100a
Power Control Module
100b
100n
235
Power Supply
234a
234b
234h
DC Parametric Unit
236
Device Under Test
264
44a
44b
44n
Per Pin/DUT
240
252
192
Temperature Controller
188
242
244
250
Stimulus
254
Response
256
239
DC Measurement Subsystem
238
248
246
Pattern Generator
258
Fail Log/ Map
233 Control
232
189
System Controller
230

Fig. 35

Fig. 36

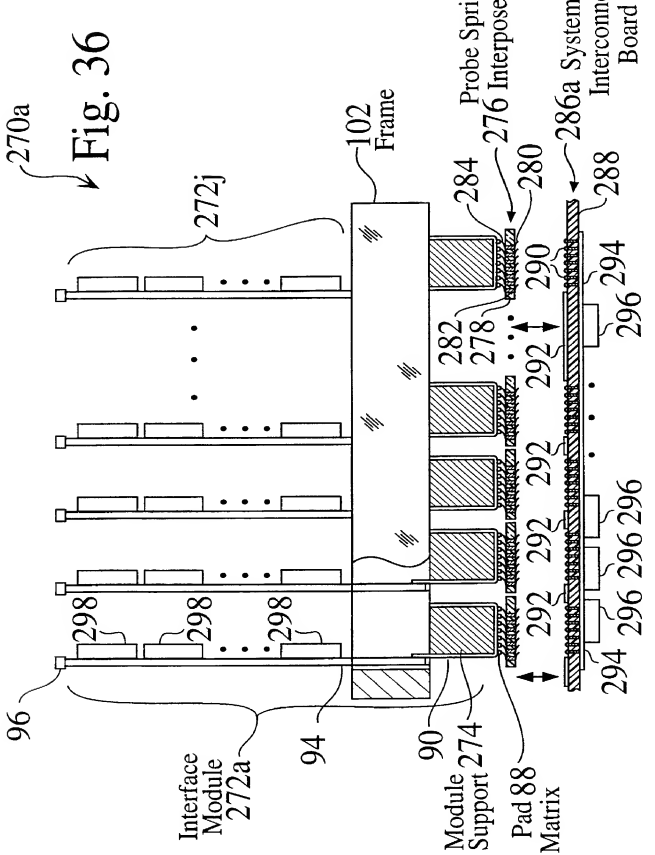
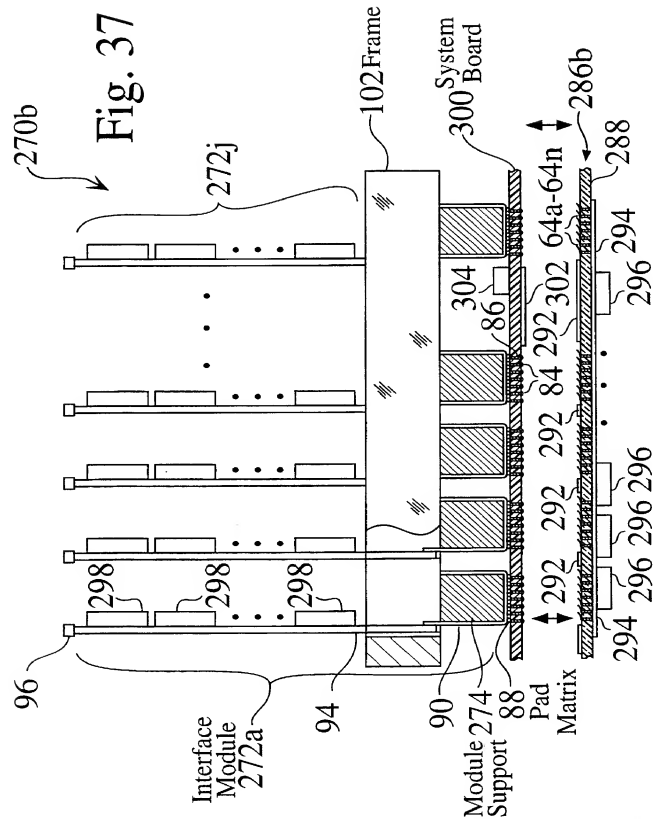

270a
272j
102
Frame
Probe Spring
276 Interposer
286a System
Interconnect
Board
284
280
288
290
294
296
282
278
292
298
96
94
90
Interface
Module
272a
Module
Support 274
Pad
Matrix
88

Fig. 37


270b
272j
102 Frame
300 System Board
286b
288
64a-64n
294
296
304
86
292
302
84
292
292
292
296
296
296
294
298
298
298
96
94
90
88
Interface Module 272a
Module Support 274
Pad Matrix

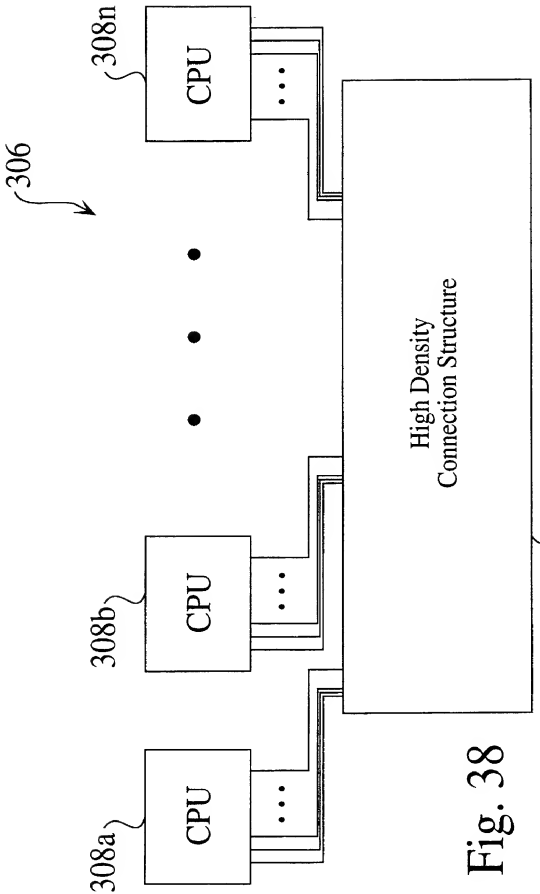


Fig. 38

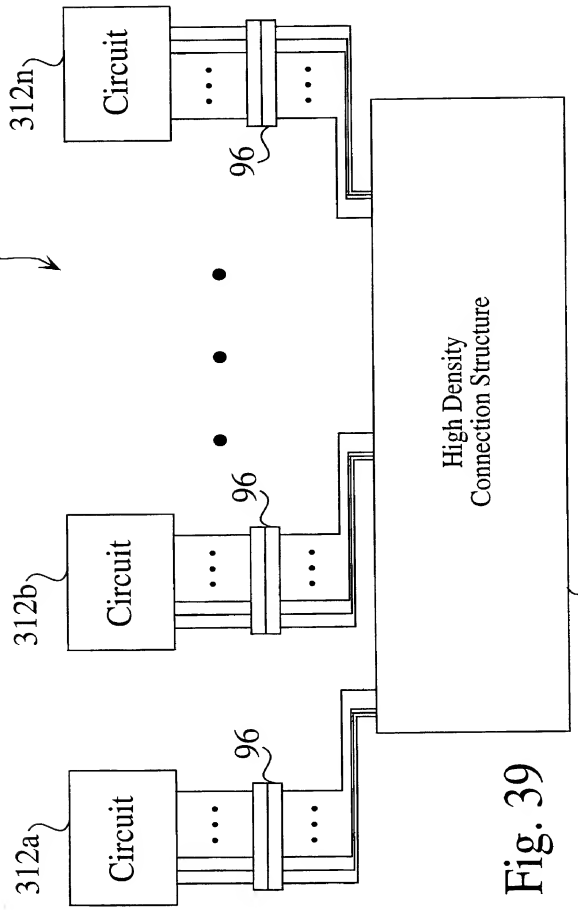

312a
Circuit
96
312b
Circuit
96
312n
Circuit
96
310
High Density
Connection Structure
270

Fig. 39

Attorney Docket No. NNEX0002

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name;

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MASSIVELY PARALLEL INTERFACE FOR ELECTRONIC CIRCUITS

the specification of which (check one) X is attached hereto, or __ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

==========

I hereby claim foreign priority benefits under Title 35, United Sates Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
PCT/US00/14768	26 May 2000		X	
Number	Country	Day/Month/Year Filed		
Number	Country	Day/Month/Year Filed		

==========

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

(4)

MICHAEL A. GLENN, Reg. No. 30,176
DONALD M. HENDRICKS, Reg. No. 40,355
KIRK D. WONG, Reg. No. 43,284
CHRISTOPHER PEIL, Reg. No. 45,005

SEND CORRESPONDENCE TO:

GLENN PATENT GROUP, 3475 Edison Way, Suite L, Menlo Park, CA 94025

==========

Attorney Docket No. NNEX0002

I hereby claim the benefit under Title 35, United States code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

60/136,637	5/27/99	PROVISIONAL - Pending
Application Ser. No.	Filing Date	Status: Patented, Pending, Abandoned

==========

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

1-00

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Inventor's signature _____ Date 8/22/01

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Post Office Address Same

Citizenship Malaysia

2-00

Full name of second or joint inventor: SAMMY MOK

Inventor's signature _____ Date Aug 23, 2001

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Post Office Address Same

Citizenship Canadian CAX